TECHNICAL MANUAL

CIRCUIT DIAGRAMS

VOLUME II

SCHEMATIC DIAGRAMS

RADAR SET TYPE AN/TPS-43E

WESTINGHOUSE ELECTIRC CORPORATION)
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INTRODUCTION

This volume contains schematic and logic diagrams for the AN/TPS-43E Radar Set. Table 1 precedes the schematic and logic diagrams and contains information pertaining to the integrated circuits used on the planar array cards and the printed circuit boards. The integrated circuit cross-reference data (table 1) is divided into five columns: assembly and part number, reference designation, specification drawing, description, and figure number.

Assembly and Part Number - This column lists the proper name of each assembly and its corresponding part number.

Reference Designation - This column identifies the respective integrated circuit by U number. This column also lists the type number of a commercial unit with similar characteristics. In most cases the integrated circuit used in the assembly is a special, specified and selected item that is only similar to the commercial unit, i.e., these units are not to be considered as replacements for those in the assembly. For exact replacement units, refer to the illustrated parts breakdown. The commercial unit part number is included in this column so that additional descriptive data may be obtained from the respective manufacturer's data book.

Specification Drawing - This column lists the Westinghouse or military specification applicable to each integrated circuit.

Description - This column contains a brief functional description of each integrated circuit.

Figure Number - This column identifies the figure number corresponding to each integrated circuit. These figures contain a schematic/logic diagram of each unit along with descriptive data and truth tables as applicable. These figures have been placed immediately after table 1.

The following tabulation provides the key to a coding scheme used to identify the source and destination of signals as they are routed into or out of a plug in unit. Within the schematics a code could exist as follows: J2. This should be interpreted to mean sheet 2 of the JATS board assembly (352D868G01).

CODE	ASSEMBLY	DWG NO.
G	Range Azimuth Gating Board Assy	352D870G01
X	Driver Board Assy	352D883G01
F	Digital Height Read-Out Board Assy	352D872G01
A	A/D Converter Board Assy	361D866G01
A	Alternate A/D Converter Board Assy	352D877G01
H1	Height Computer 1 Board Assy	352D862G01
H2	Height Computer 2 Board Assy	352D863G01
E	Height Evaluator Board Assy	352D865G01
EM	Evaluator Memory Board Assy	352D867G01
B	BITE Board Assy	352D861G01
D/A	D/A Converter Board Assy	352D881G01
J	JATS Board Assy	352D868G01
S1	Synchronizer 1 Board Assy	352D859G01
S2	Synchronizer 2 Board Assy	325D860G01
C	Channel Control Board Assy	352D858G01
I	Dual Integrator Board Assy	352D857G01
M	8-Bit Memory Board Assy	352D879G01
K	Receiver Control Board Assy	352D871G01
D	Canceller/Decoder Board Assy	352D856G01
P	U.S.P. Control Panel	353D273G01
SG	Signal Generator (Freq. Gen.)	353D985G01

EFFECTIVITY. Effectivity codes are used, as applicable, to insure the T.O. remains compatible with the equipment both before and after a hardware modification.

This manual is effective for all radar sets bearing Westinghouse serial numbers 2501 and subsequent. Effectivities are defined in code if portions of the manual reflect changes made to the basic model. In most cases, paragraphs affected by a major change have been completely rewritten to incorporate the change, and the new paragraph bears the proper effectivity code designations. With major changes of this type, where old paragraphs are no longer applicable to the modified equipment, alternate effectivity code designations are used to indicate that a particular paragraph is to be disregarded. In cases where a change merely requires additional text for proper coverage, the alternate effectivity code designations are not used. Text that contains no effectivity code designation should be considered effective for all radar sets bearing Westinghouse serial numbers 2501 and subsequent. The following table lists the proper effectivity code, the engineering change proposal (ECP) and/or time compliance technical order (TCTO) authorizing the modification of such units, the part number of the modified unit, and a brief description of the specific system difference after incorporation of the modification.

EFFECTIVITY CODES

Effectivity Code	ECP	TCTO	LRU Part No.	Description of Change
Ⓐ	001	31P3-2TPS43-564	356D394G01	Circuit change to the Search/MTI IF Receiver card that increases the range of the MTI GAIN adjustment.
Ⓑ	002	31P3-2TPS43-565	347D333G01	Circuit change to the RF Amplifier that improves the reliability of the reset function.
Ⓒ	003	31P3-2TPS43-563	352D969G02	Circuit change to the Height IF Receiver card that eliminates noise on the sample pulse and increases the range of the LOG SLOPE adjustment.
Ⓓ	004	31P3-2TPS43-566	139C413G01 and 139C384G01	Circuit change to the Fan Monitor board to increase the ac filtering action and thus improve the dc response of the board.
Ⓔ	005	31P3-2TPS43-567	353D345	Circuit change to the 1A7 Power Distribution Panel to filter power supply transients more effectively to reduce false triggering.
Ⓕ	007	-	347D333G01	Circuit change to the RF Amplifier that improves operational reliability of the assembly.
Ⓖ	-	31P3-2TPS43-561 and 562	360D481G01	Addition of two decoder expander units to provide for additional passive decoding capabilities. Also adds the shelter cabling necessary to interface the TPS-43E and the TSQ-61.

EFFECTIVITY CODES (Continued)

Effectivity Code	ECP	TCTO	LRU Part No.	Description of Change
H	008	31P3-2TPS43-568	353D379G01	Addition of a MAIN POWER SAFETY INTERRUPT switch.
I	009	-	132C777G01	Replacement of sensor resistor string assembly 1A17A2 with a more reliable assembly.
J	010	31P3-2TPS43-572	332D885G01	Install seven 3dB attenuators at input ports of stalo power divider to improve performance of microwave distribution box.
K	013	-	352D856	Addition of a wire to improve stability of U71 and thereby improve LRU reliability.
L	016	-	352D934	Component change on LRU to improve reliability of board.
M	017	-	356D394G02	Component changes on LRU to improve operating characteristics of board.
N	018	31P3-2TPS43-575	355D002G01	Component changes on LRU to improve operating characteristics of board.
O	019	-	352D934	Component change on LRU to stabilize IF monitor circuit.
P	022	-	361D866	Component change on LRU due to unavailability of component.

Table 1. Integrated Circuit Cross-Reference Data

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
15-Volt Regulator and Range-Azimuth Control 338D664G01	U1-3 (54121)	128C823H12	Monostable Multivibrator	1
Interface Buffer 338D697G01	U1 (5404)	128C821H04	Hex Inverter	2
	U2 (5400)	128C821H01	Quad 2-Input Positive NAND Gate	3
IFF Switch Driver 338D942G01	U1 (54121)	128C823H12	Monostable Multivibrator	1
	U2 (710)	128C213H01	Differential Comparator	4
Quantizer-Oscillator 351D840G01	U1, 5 (710)	581R500H84	Differential Comparator	4
	U2 (54121)	M38510/ 01201BCB	Monostable Multivibrator	1
	U3 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U4, 8-13, 15-19 (NH-0002)	649A819H01	Current Amplifier, Analog	6
	U7 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7
	U14 (5407)	581R500J44	Hex Buffer/ Driver W/Open Collector, H.V.	8
Canceller-Decoder 352D856G01	U0,9,10, 12,19,40, 97 (U7B-9322)	659A815H02	Quad 2-Input MUX	9

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Canceller-Decoder 352D856G01 (Continued)	U3,5,6,14-16,20,21,23,25,26,31,32,33,35,63,72,73,75,83,85 (54283)	581R646H01	4-Bit Binary Full Adder W/ Fast Carry	10
	U8,17,18,27-29,38,39, (SN-54175)	578R995H01	Quad D-Type F-F	11
	U36,53,94,99 (U6A-5404)	578R558H02	Hex Inverter	2
	U42,44,45,78,79 (U6A-5405)	578R560H02	Hex Inverter, Open Collector	2
	U47,48,71 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U49 (5437)	582R722H01	Quad 2-Input Positive NAND Gate Buffer	3
	U51,61 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U54,56,57,80,82,90 (U7B-9324)	649A818H02	5-Bit Comparator	15
	U64,65,67,68,76,77 (54153)	581R019H01	Dual 4-Input MUX	16
	U58,59 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Canceller-Decoder 352D856G01 (Continued)	U43,55	M8340102 M102JB	Resistor Network	30
Dual Integrator 352D857G01	U4,7,14,17, 31-34,37, 38,64,67, 74,77,91- 94,97,98 (U7B-9322)	649A815H02	Quad 2-Input MUX	9
	U5,15,21, 24,25,27, 28,65,75, 81,84,85, 87,88, (54283)	581R646H01	4-Bit Binary Full Adder W/Fast Carry	10
	U6,16,29, 39,66,76, 89,99 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U8,9,12, 13,18,19, 22,23,68, 69,72,73, 78,79,82, 83 (54153)	581R019H01	Dual 4-Input MUX	16
	U26,40,53, 63,86 (U6A-5404)	578R558H02	Hex Inverter	2
	U52 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U36,37,95, 96 (U7B-9324)	649A818H02	5-Bit Com- parator	15
	U43-46,54- 56 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Dual Integrator 352D857G01 (Continued)	U47,48,57, 58 (U6A-5405)	578R560H02	Hex Inverter, Open Collector	2
	U49 (5437)	582R722H01	Quad 2-Input Positive NAND Gate Buffer	3
	U42,50,51	M8340102 M102JB	Resistor Network	30
Channel Control 352D858G01	U5,15,27, 46,47,52, 53,89,99 (U7B-9322)	649A815H02	Quad 2-Input MUX	9
	U6,16,25 (U7B-9324)	649A818H02	5-Bit Comparator	15
	U7,82 (5410)	M38510/ 00103BCB	Triple 3-Input NAND Gate	17
	U17 (U6A-5430)	578R613H02	8-Input NAND Gate	18
	U28,66 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U29,77,88, 93 (IM-5610)	581R137H01	256-Bit Bipolar PROM, Tri-State Output	19
	U33 (5486)	M38510/ 00701BCB	Quad 2-Input Exclusive OR Gate	20
	U35,73,55 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U39,48,68, 78,79,45 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Channel Control 352D858G01 (Continued)	U44,56,57 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U49 (54S140)	581R548H02	Dual 4-Input NAND Gate Line Driver	7
	U8,18,19, 43,75,76, 83 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U54 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U63,64 (SN-54175)	578R995H01	Quad D-Type F-F	11
	U65 (U6A-5405)	578R560H02	Hex Inverter, Open Collector	2
	U67,94,95, 96,97 (54153)	581R019H01	Dual 4-Input MUX	16
	U69 (54148)	649A817H03	10-Line Decimal-to-4-Line BCD Decoder	23
	U9,36,74, 86,87,98 (U6A-5404)	578R558H02	Hex Inverter	2
	U34,71,72 84,85 (54161)	581R500H36	Binary Counter	24
	U58,59 (54283)	581R646H01	4-Bit Binary Full Adder W/ Fast Carry	10

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Channel Control 352D858G01 (Continued)	U37,38	581R871H41	Resistor Network	35
	U41,51, 61,62	M8340102 M102JB	Resistor Network	30
Synchronizer No. 1 352D859G01	U0,21,23, 25,62,64 (54161)	581R500H36	Binary Counter	24
	U1,2 (54153)	581R019H01	Dual 4-Input MUX	16
	U3,66 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U4 (IM-5610)	581R137H01	256-Bit Bipolar PROM, Tri-State Output	19
	U5,78 (5410)	M38510/ 00103BCB	Triple 3-input NAND Gate	17
	U6,7,16, 41,60,65, 82,87,94 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered Flip-Flop	21
	U9,18,43-45,69,79, 89,99 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U10-12,15, 30-33,35, 50-53,70-73,75,83, 84 (5425)	M38510/ 00403BCB	Dual 4-Input NOR Gate W/ Strobe	25
	U13,14 (U7B-9324)	649A818H02	5-Bit Comparator	15

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Synchronizer No. 1 352D859G01 (Continued)	U17,20,40, 88 (U6A-5404)	578R558H02	Hex Inverter	2
	U27-29,38 39 (54S140)	581R548H02	Dual 4-Input NAND Gate Line Driver	7
	U22,24,34, 61,63,74 (5442)	M38510/ 01001BEB	BCD-to-Decimal Decoder/Driver	26
	U26,36,46 (54S112)	581R136H01	Dual J-K Neg. Edge-Triggered F-F	27
	U48 (54S00)	581R135H01	Quad 2-Input Positive NAND Gate	3
	U54,56,58, 67 (54164)	682R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U76 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U77 (9615)	581R271H02	Dual Line Receiver	28
	U81 (5438)	M38510/ 00303BCB	Quad 2-Input Positive NAND Gate Buffer W/Open Collector	29
	U85 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U37,47 (93S16)	582R241H01	4-Bit Binary Counter, Edge-Triggered, Fully Synchronized	24

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Synchronizer No. 1 352D859G01 (Continued)	U8,86	M8340102 M102JB	Resistor Network	30
	U49	581R871H41	Resistor Network	35
Synchronizer No. 2 352D860G01	U6,7,15, 18,29,31, 37,38,43, 46-48,52, 53,64,76, 79,85 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U8,9,49, 69,81 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U21 (54283)	581R646H01	4-Bit Binary Full Adder W/ Fast Carry	10
	U13,14,19 24,25,39, 41,42,51, 61,62,68, 78,83 (54161)	581R500H36	Binary Counter	24
	U16,27,33-35 (5425)	M38510/ 00403BCB	Dual 4-Input NOR Gates W/ Strobe	25
	U17,44,54, 57,58,88 (U6A-5404)	578R558H02	Hex Inverter	2
	U22,32 (U7B-9324)	649A818H02	5-Bit Comparator	15
	U23,28,36, 45,77,86 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Synchronizer No. 2 352D860G01 (Continued)	U26,56,63, 75 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U55,84 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U59 (U6A-5430)	578R613H02	8-Input NAND Gate	18
	U65 (5410)	M38510/ 00103BCB	Triple 3-Input NAND Gate	17
	U66,87 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7
	U67 (5442)	M38510/ 01001BEB	BCD-to-Decimal Decode/ Divider	26
	U71 (54123)	581R500H89	Dual Monostable Multivibrator	31
	U72 (IM-5610)	581R137H01	256-Bit Bipolar PROM, Tri-State Output	19
	U89 (54S140)	581R548H02	Dual 4-Input NAND Gate Line Driver	7
	U91 (5432)	581R610H01	Quad 2-Input Positive OR Gate	33
	U73 (SN-54174)	578R995H02	Hex D-Type F-F	12

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Synchronizer No. 2 352D860G01 (Continued)	U74 (54S00)	581R135H01	Quad 2-Input Positive NAND Gate	3
	U82 (5438)	M38510/ 00303BCB	Quad 2-Input Positive NAND Gate Buffer W/Open Collector	29
	U30,99	M8340102 M102JB	Resistor Network	30
BITE 352D861G01	U5-7,13-17,75 (54153)	581R019H01	Dual 4-Input MUX	16
	U8,57-59,68,79 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U9 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U27-29, 36,67,88 (U6A-5404)	578R558H02	Hex Inverter	2
	U37,87 (5410)	M38510/ 00103BCB	Triple 3-Input NAND Gate	17
	U38,63,64 85 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U39,U66 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U44 (5402)	M38510/ 00401BCB	Quad 2-Input NOR Gate	32
	U46 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
BITE 352D861G01 (Continued)	U54,86 (5432)	581R610H01	Quad 2-Input Positive OR Gate	33
	U56 (54148)	649A817H03	10-Line Decimal-to-4-Line BCD Decoder	23
	U65 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U74 (54195)	582R723H02	4-Bit Shift Register	34
	U76 (54161)	581R500H36	Binary Counter	24
	U78,98,99 (5438)	M38510/ 00303BCB	Quad 2-Input Positive NAND Gate Buffer W/ Open Collector	29
	U77 (IM-5610)	581R137H01	256-Bit Bipolar PROM, Tri-State Output	19
	U96,97 (SN-54175)	578R995H01	Quad D-Type F-F	11
	U18,19,69	581R871H41	Resistor Network	35
	U48,49,89	M8340102 M102JB	Resistor Network	30
Height Computer No. 1 352D862G01	U1,2,11, 12,50,60, 84,95 (U7B-9324)	649A1818H02	5-Bit Comparator	15
	U5,15-17, 35 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Height Computer No. 1 352D862G01 (Continued)	U6,54,77 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U7 (SN-54175)	578R995H01	Quad D-Type F-F	11
	U8,9,36, 37,41,42, 46,47,57, 58,63,64, 83,93,94 (U7B-9322)	649A815H02	Quad 2-Input MUX	9
	U10 (5486)	M38510/ 00701BCB	Quad 2-Input Exclusive OR Gate	20
	U18,24 (5410)	M38510/ 00103BCB	Triple 3-Input NAND Gate	17
	U0,3,4, 20,78 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U21,22,68 (U6A-5404)	578R558H02	Hex Inverter	2
	U23 (5402)	M38510/ 00401BCB	Quad 2-Input NOR Gate	32
	U25-27 (U6A-5430)	578R613H02	8-Input NAND Gate	18
	U28,45 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7
	U30-33,43, 44,51-53, 55,56,74-76,85,86, 96 (54283)	581R646H01	4-Bit Binary Full Adder W/ Fast Carry	10

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Height Computer No. 1 352D862G01 (Continued)	U34,40 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U38,39,48, 49 (54153)	581R019H01	Dual 4-Input MUX	16
	U14,61,62, 65-67 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U73 (5432)	581R610H01	Quad 2-Input Positive OR Gate	33
	U59	581R871H41	Resistor Network	35
	U87-89,97, 98 (9615)	581R271H02	Dual Differential Line Receiver	28
	U29,69	M8340102 M102JB	Resistor Network	30
Height Computer No. 2 352D863G01	U6-9,18, 19,28,29, 39 (9615)	581R271H02	Dual Line Receiver	28
	U17,26,58, 69,79 (U7B-9322)	649A815H02	Quad 2-Input MUX	9
	U24,38,47, 48,57 (54161)	581R500H36	Binary Counter	24
	U25,77 (U6A-5404)	578R558H02	Hex Inverter	2
	U32,33 (U7B-9324)	649A818H02	5-Bit Comparator	15

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Height Computer No. 2 352D863G01 (Continued)	U34,37,87 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U35,82-85 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U36,46,56, 66,67 (54153)	581R019H01	Dual 4-Input MUX	16
	U42-44,52-54,70-75 (5483)	581R646H01	4-Bit Binary Full Adder W/ Fast Carry	10
	U45,55,65 (54195)	582R723H02	4-Bit Shift Register	34
	U59,78 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U61-64,94, 95 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U68 (5410)	M38510/ 00103BCB	Triple 3-Input NAND Gate	17
	U76,86 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U88,89 (U6A-5403)	578R559H02	Quad 2-Input NAND Gate, Open Collector	29
	U97,99 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U16,49	581R871H41	Resistor Network	35

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Height Computer No. 2 352D863G01 (Continued)	U14,15,27	M8340102 M102JB	Resistor Network	30
Height Evaluator 352D865G01	U2,11,12, 35,41,45, 51 (U7B-9324)	649A818H02	5-Bit Comparator	15
	U5,24,64, 72 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U14,27,73 83 (U6A-5404)	578R558H02	Hex Inverter	2
	U15,82,95 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U18,25,28, 38,48,58, 68 (5486)	M38510/ 00701BCB	Quad 2-Input Exclusive OR Gate	20
	U19,29,37, 39,43,44, 47,49,53-55,57,59, 65,67,69 (54283)	581R646H01	4-Bit Binary Full Adder W/ Fast Carry	10
	U20,30,75, 92 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U22,81,94 (5410)	M38510/ 00103BCB	Triple 3-Input NAND Gate	17
	U40,50 (U6A-5403)	578R559H02	Quad 2-Input NAND Gate, Open Collector	29

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Height Evaluator 352D865G01 (Continued)	U42,52,88, 89,98,99 (SN-54175)	578R995H01	Quad D-Type F-F	11
	U46 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7
	U87,96,97 (U7B-9322)	649A815H02	Quad 2-Input MUX	9
	U21,34,74, 76-79,84, 91 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U93 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U56	M8340102 M102JB	Resistor Network	30
	U85	581R871H41	Resistor Network	35
Evaluator Memory 352D867G01	U56,63,73, 93 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U5,16,26, 32,37,45, 62,72,83 (U6A-5404)	578R558H02	Hex Inverter	2
	U15,44,92 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U34,53,54 82 (5410)	M38510/ 00103BCB	Triple 3-Input NAND Gate	17
	U52 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Evaluator Memory 352D867G01 (Continued)	U33,39 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U49 (5486)	M38510/ 00701BCB	Quad 2-Input Exclusive OR Gate	20
	U47,55,64, 84,94 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U75,76,85, 86,95,96 (54153)	581R019H01	Dual 4-Input MUX	16
	U43,77,87, 97 (54161)	581R500H36	Binary Counter	24
	U74 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U88,89,98, 99 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U67-69, 78,79 (SN-54175)	578R995H01	Quad D-Type F-F	11
	U9,48 (54180)	581R825H01	8-Bit Odd/ Even Parity Generator/ Checker	36
	U65,66 (U7B-9322)	649A815H02	Quad 2-Input MUX	9
	U58,59 (U7B-9324)	649A818H02	5-Bit Comparator	15

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Evaluator Memory 352D867G01 (Continued)	U2-4,6-8, 12-14,17-19,23-25, 27-29,35, 36,38,46 (AM-2833)	649A888H01	1024-Bit Static Shift Register	37
	U42	581R871H41	Resistor Network	35
	U57	M8340102 M102JB	Resistor Netowrk	30
JATS 352D868G01	U2,3,31-35,83,84 (5410)	M38510/ 00103BCB	Triple 3-Input NAND Gate	17
	U4,30,72 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U5,40,50, 60,70 (U7B-9324)	649A818H02	5-Bit Comparator	15
	U6 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U7,10-13, 20-23,42-45,52-55, 62,87,88 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U8,9,96 (U7B-9322)	649A815H02	Quad 2-Input MUX	9
	U14,15,24, 25,36-39, 46-49,63, 64,73,74 (SN-54175)	578R995H01	Quad D-Type F-F	11

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
JATS 352D868G01 (Continued)	U16,56-69, 85,86 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U18,19,28, 29 (U6A-5403)	578R559H02	Quad 2-Input NAND Gate, Open Collector	29
	U26,89 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U41,82 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U51 (5486)	M38510/ 00701BCB	Quad 2-Input Exclusive OR Gate	20
	U61,71 (5442)	M38510/ 01001BEB	BCD-to-Decimal Decode/Driver	26
	U66-69,76-79 (5438)	M38510/ 00303BCB	Quad 2-Input Positive NAND Gate Buffer W/ Open Collector	29
	U81 (54161)	581R500H36	Binary Counter	24
	U93-95 (U6A-5404)	578R558H02	Hex Inverter	2
	U65,75	M8340102 M302JB	Resistor Network	30
	U17,27	M8340102 M102JB	Resistor Network	30
RAG 352D870G01	U13,19,45 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
RAG 352D870G01 (Continued)	U98 (5402)	M38510/ 00401BCB	Quad 2-Input NOR Gate	32
	U18,49,58, 59,73,77 (U6A-5404)	578R558H02	Hex Inverter	2
	U33,48,57, 96 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U85 (5410)	M38510/ 00103BCB	Triple 3-Input Positive NAND Gate	17
	U97 (5432)	581R610H01	Quad 2-Input Positive OR Gate	33
	U9,39,69, 79,89 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U21,54,86 (5486)	M38510/ 00701BCB	Quad 2-Input Exclusive OR Gate	20
	U8,24,26, 32,46, 47,67,74, 88 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U38 (54153)	581R019H01	Dual 4-Input MUX	16
	U4-7,14-17, 22,23,27, 36,42,55, 56,65,66, 75,76 (54161)	581R500H36	Binary Counter	24

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
RAG 352D870G01 (Continued)	U2,12,28, 34,35,37 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U40,41,61, 62 (SN-54174)	578R995H02	Hex D-Type F-F	12
	U43,44,63, 64,83,84 (U7B-9324)	649A818H02	5-Bit Comparator	15
	U99 (9615)	581R271H02	Dual Line Receiver	28
	U3,25,87, 95	M8340102 M102JB	Resistor Network	30
	U29,68,78	581R871H41	Resistor Network	35
Receiver Control 352D871G01	U1,6,8,10 21,27,57, 67 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U2,12,15, 24, (5410)	M38510/ 00103BCB	Triple 3-Input Positive NAND Gate	17
	U14,18,25, 28,38,46, 71,78 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U16,17,26, 35,52,75, 83 (U6A-5404)	578R558H02	Hex Inverter	2
	U23,89,96 (5432)	581R610H01	Quad 2-Input Positive OR Gate	33

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Receiver Control 352D871G01 (Continued)	U30,31 (SN-54175)	578R995H01	Quad D-Type F-F	11
	U32,48 (54148)	649A817H03	10-Line Decimal-to-4-Line BCD Decoder	23
	U34 (5442)	M38510/ 01001BEB	BCD-to-Decimal Decode/ Driver	26
	U37,64,93 (5402)	M38510/ 00401BCB	Quad 2-Input Positive NOR Gate	32
	U41,51 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7
	U43,66 (54164)	582R723H03	8-Bit Parallel-Out Serial Shift Register	14
	U49,68,69 (5437)	M38510/ 00302BCB	Quad 2-Input Positive NAND Gate Buffer	3
	U50,55,61, 65,77 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U53,74 (54161)	581R500H36	Binary Counter	24
	U84,88,97 (U7B-9322)	649A815H02	Quad 2-Input MUX	9
	U19,29	M8340102 M102JB	Resistor Network	30
	U79,89,99	581R871H41	Resistor Network	35

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Digital Height Readout 352D872G01	U2,12,22, 62,72 (54192)	581R500J53	UP/DN BCD Counter	38
	U3,13,23, 33,42,44, 52,54,61, 64,71,81, 91 (U7B-9324)	649A818H02	5-Bit Comparator	15
	U4,31,46, 66,67,75, 86,87,95, 96 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U5,34,47, 56,63,93 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U14,36,57, 59,69,79, 94 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U24,26,58, 73,89,97 (U6A-5404)	578R558H02	Hex Inverter	2
	U35,83 (5402)	M38510/ 00401BCB	Quad 2-Input NOR Gate	32
	U37,84,88 (5410)	578R574H03	Triple 3-Input NAND Gate	17
	U32,43,45, 53,55,65, 82,92 (54193)	581R500J12	4-Bit UP/DN Binary Counter	39
	U68 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Digital Height Readout 352D872G01 (Continued)	U38,78 (SN-54174)	578R995H02	Hex D-Type Flip-Flop	12
	U48 (5432)	581R610H01	Quad 2-Input OR Gate	33
	U15,51	M8340102 M302JB	Resistor Network	30
	U25	M8340102 M102JB	Resistor Network	30
A/D Converters 361D866 and 352D877	U1,5,9, 27 (MC-10505)	581R688H07	Triple 2-3-2 Input OR/NOR Gate	40
	U2,6-8, 10,11 (10631)	138C439H01	Dual D-Type Master-Slave F-F	41
	U3,12-20 (95029)	138C566H01	J-K F-F, Edge-Triggered	42
	U4 (MC-10504)	581R688H08	Quad 2-Input AND Gate	13
	U21-26 (MC-1268)	583R357H02	Level Translator, ECL to TTL	43
	*U21-26 (MC-1268)	138C461H01	Level Translator, ECL to TTL	43.1
	U28 (AM-685)	581R709H02	Comparator, High-Speed, ECL Outputs	44
	U29 (DG-188AA)	578R823H03	Analog Gate, H.S. DPST	45
	U30,31 (LH-0033G)	581R684H01	Amplifier Buffer, Analog	46
	U32-34 (5475)	578R644H02	Quad Bistable Latch	47

* Used on 352D877

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
8-Bit Memory 352D879G01	U1 (U6A-5403)	578R559H02	Quad 2-Input NAND Gate, Open Collector	29
	U2-4,17, 18,31,32, 45,46 (MHQ-3725)	649A808H01	Quad Driver	48
	U5-9,11-14, 16,19-23, 25-28,30, 33-37,39-42,44,47-51,53-56, 58 (1404)	138C177H01	1024-Bit Dynamic Shift Register	49
	U15,29,43, 57 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U59-66 (1402)	581R228H01	Quad 256-Bit Dynamic Shift Register	50
D/A Converter 352D881G01	U1-3,6, 8 (5406)	581R500H71	Hex Inverter Buffer/Driver with Open Collector, High Voltage Outputs	51
	U4 (741)	581R500J17	Linear OP AMP (8 Lead Can)	22
	U5,7,9-14 (NH-0002)	649A819H01	Current Amp	6
Driver 352D883G02	U1,12 (5406)	581R500H71	Hex Inverter, Open Collector HV	51

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Driver 352D883G02 (Continued)	U15 (9615)	581R271H02	Dual Line Receiver	28
	U2-11,13, 14 (NH-0002)	649A819H01	Current Amp	6
Video Output 352D885G01	U1,3 (DG-188AA)	578R823H03	Analog Gate, H.S. DPST	45
	U2 (HA2-2620-8)	142C675H01	Analog OP AMP	53
	U4-9 (NH-0002)	649A819H01	Current Amp	6
Video Amplifier 352D887G01	U1 (MC-1520G)	649A821H01	Differential Video Amplifier	54
Squaring Circuit 352D889G01	U1 (54S00)	581R135H01	Quad 2-Input Positive NAND Gate	3
Beam Pair Selector 352D937G01	U2,3,5,6, 8,9,11,12, 14,15 (711)	578R642H01	Dual Linear Comparator	55
	U1,4,7,10, 13 (HA2-2620-8)	142C675H01	OP AMP	53
	U16 (U6A-5404)	578R558H02	Hex Inverter	2
Summing Amplifier and Electronic Switch 352D963G01	U1-3 (747)	582R728H02	Dual Linear OP AMP	56
	U4 (5410)	581R500J26	Triple 3-Input NAND Gate	17

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Summing Amplifier and Electronic Switch 352D963G01 (Continued)	U5 (5406)	581R500H71	Hex Inverter, Open Collector HV	51
	U6-9 (LM-318)	581R923H02	Analog OP AMP	57
Height IF Receiver 352D969G02	U3,5,6 (HA2-2620-8)	142C675H01	Analog OP AMP	53
	U4,7 (110)	581R710H02	OP AMP, Voltage Follower	58
Beam Subtractor 352D973G01	U1,4,7,10, 13,19 (HA2-2620-8)	142C675H01	Analog OP AMP	53
	U2,5,8,11, 14,16 (DG-182AA)	578R823H05	Dual Analog Gate, HS SPST Switch	59
	U3,6,9,12, 15 (110)	581R710H02	OP AMP, Voltage Follower	58
	U17,18 (741)	M38510/ 10101BCB	Linear OP AMP	52
	U20 (NH-002)	649A819H01	Current Amp	6
	U21 (710)	581R500H84	Differential Comparator	4
Peak Selector 352D975G01	U1 (DG-182AA)	578R823H05	Dual Analog Gate HS SPST Switch	59
	U2,15 (HA2-2620-8)	142C675H01	Analog OP AMP	53

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Peak Selector 352D975G01 (Continued)	U3,7 (741)	M38510/ 10101BCB	Linear OP AMP	52
	U4,8 (710)	581R500H84	Differential Comparator	4
	U5,13 (U7B-9602)	578R601H01	Dual Monostable Multivibrator, Digital-to-TTL	60
	U6 (54S140)	581R548H02	Dual 4-Input NAND Gate Line Driver	7
	U9 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U10,14 (5410)	M38510/ 00103BCB	Triple 3-Input Positive NAND Gate	17
	U11 (U6A-5404)	578R558H02	Hex Inverter	2
	U12 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
Sidelobe Blanker 352D980G01	U1 (710)	581R500H84	Differential Comparator	4
	U2 (U7B-9602)	578R601H01	Dual Monostable Multivibrator, Digital-to-TTL	60
	U3,4 (3705)	581R803H01	Analog Multiplex Switch, 8-Channel MOS	61
	U5 (741)	M38510/ 10101BCB	Linear OP AMP	

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Sidelobe Blanker 352D980G01 (Continued)	U6 (HA2-2620-8)	142C675H01	Analog OP AMP	53
	U7 (NH-0002)	649A819H01	Current Amp	6
Search/MTI IF Receivers 356D394G01 356D394G02	U1,2,5 (HA2-2620-8)	142C675H01	Analog OP AMP	53
	U3,4 (741)	M38510/ 10101BCB	Linear OP AMP	52
	U6 (NH-0002)	649A819H01	Current Amp	6
JATS/Weather Receiver 352D984G01	U1,3 (1550)	578R765H02	Analog AMP, RF-IF	62
	U2,5 (HA2-2620-8)	142C675H01	Analog OP AMP	53
	U4 (110)	581R710H02	OP AMP, Voltage Follower	58
COHO Splitter/STC Generator 352D986G01	U1-9 (741)	M38510/ 10101BCB	Linear OP AMP	52
Defruiter Control/ Memory 352D994G01	U9,68,78 (5400)	578R553H02	Quad 2-Input Positive NAND Gate	3
	U19 (5402)	M38510/ 00401BCB	Quad 2-Input NOR Gate	32
	U27,86 (SN-5408J)	578R988H01	Quad 2-Input AND Gate	5
	U26 (U6A-5420)	578R562H02	Dual 4-Input NAND Gate	7

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Defruiter Control/ Memory 352D994G01 (Continued)	U8,18,87 (54109)	581R817H01	Dual J-K Bar Positive Edge-Triggered F-F	21
	U77 (54121)	M38510/ 01201BCB	Monostable Multivibrator	1
	U35,45,55, 65,74,84 (54193)	581R500J12	4-Bit Up/Down Binary Counter	39
	U36-39,46-49,56-59 (AM-2833)	649A888H01	1024-Bit Static Shift Register	37
	U28	M8340102 M102JB	Resistor Network	30
IFF Trigger Generator 355D014G01	U1-3 (54161)	581R500H36	Binary Counter	24
	U4-9 (U7B-9324)	649A818H02	5-Bit Comparator	15
	U10 (5400)	578R533H02	Quad 2-Input Positive NAND Gate	3
	U11 (5406)	581R500H71	Hex Inverter, Open Collector HV	51
	U16 (9615)	581R271H02	Dual Line Receiver	28
	U12-15,17-21 (NH-0002)	649A819H01	Current Amp	6
Video Driver 355D035G01	U1-15 (NH-0002)	649A819H01	Current Amp	6

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Module or Integrated Circuit				
Assembly and Part No.	Ref. Des.	Spec. Dwg.	Description	Fig. No.
Headset Amplifier 355D049G01	U1-6 (741)	M38510/ 10101BGC	Linear OP AMP, 8-Lead Can	22
Oscillator 355D055G01	U1-3 (555)	142C516H01	Analog Timer	63
Speaker Amplifier 355D059G01	U1-3 (741)	M38510/ 10101BGB	Linear OP AMP, 8-Lead Can	22
Troposcatter 355D064G01	U1-4 (555)	142C516H01	Analog Timer	63
20 Hz Ringout 355D071G01	U1 (555)	142C516H01	Analog Timer	63
Timing Logic 355D072G01	U3,10,11, 20,21,30-35,45,61, 62 (5400)	128C821H01	Quad 2-Input Positive NAND Gate	3
	U1,46,57 63,69,96 (5404)	128C821H04	Hex Inverter	2
	U2,16,26, 28,44,48, 49,77 (5420)	128C821H07	Dual 4-Input NAND Gate	7
	U4,5,9 29,47,54, 58,59,67, 68,72,95 (5473)	128C823H02	Dual J-K Master-Slave F-F	64
	U90-92 (5475)	128C830H02	4-Bit Bi-stable Latch	65
	U19 (5486)	128C821H12	Quad 2-Bit Input Exclusive OR Gate	70

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Module or Integrated Circuit				
Assembly and Part No.	Ref. Des.	Spec. Dwg.	Description	Fig. No.
Timing Logic 355D072G01 (Continued)	U73,83,84, 93 (5490)	128C955H01	Decade Counter	67
	U18,27,38, 39,71,78, 79,89 (54121)	128C823H12	Monostable Multi-vibrator	1
	U40-43,55, 65,75,80-82,85 (7200)	128C921H01	4-Bit Com-parator	68
	U6-8,12, 15,22,25, 53,56 (54193)	128C830H14	4-Bit UP/DN Binary CTR	39
	U13,14,23, 24,50-52, 66,86,76 (54192)	128C830H13	4-Bit UP/DN Decade CTR	38
	U94 (5493)	128C830H05	4-Bit Binary Counter	69
Azimuth Logic 355D074G01	U25,35,45, 49,58,68, 77,78,87-89,97-99 (5400)	128C821H01	Quad 2-Input Positive NAND Gate	3
	U13,22,23, 32,33,42-44,46,47, 48,51 (5403)	128C821H03	Quad 2-Input NAND Gate, Open Collector Outputs	29
	U14,15,36, 37,61,79, 83-85 (5404)	128C821H04	Hex Inverter	2

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Azimuth Logic 355D074G01 (Continued)	U24,57,71, 93,94 (5420)	128C821H07	Dual 4-Input NAND Gate	7
	U39,59,67, 86,95,96 (5473)	128C823H02	Dual J-K Master-Slave F-F	64
	U8,9,18, 19,28,29, 69,80,82, 90,92 (5475)	128C830H02	4-Bit Bistable Latch	65
	U6,16,26, 38 (5483)	128C830H03	4-Bit Binary Full Adder	66
	U3-5,7,17, 27 (54H87)	128C830H04	4-Bit True Complement, Zero/One Element	71
	U81,91 (5490)	128C955H01	Decade Counter	67
	U34,54,64, 74 (5493)	128C830H05	4-Bit Binary CTR	69
	U53,55,63, 65,73,75 (7200)	128C921H01	4-Bit Comparator	68
	U52,56,62, 66,72,76 (54193)	128C830H14	4-Bit UP/DN Binary CTR	39
	U2,12 (5406)	128C829H01	Hex Inverter, Open Collector	51
	U41 (MK-007)	138C061H03	256-4 Bit ROM, Static	72

Table 1. Integrated Circuit Cross-Reference Data (Continued)

Assembly and Part No.	Module or Integrated Circuit Ref. Des.	Spec. Dwg.	Description	Fig. No.
Azimuth Logic 355D074G01 (Continued)	U31 (MK-008)	138C061H04	256-4 Bit ROM, Static	73
	U21 (MK-009)	138C061H05	256-4 Bit ROM, Static	74
	U1 (MK-010)	138C061H06	128-8 Bit ROM, Static	75

CROSS REFERENCE INDEX LIST

CROSS REFERENCE INDEX LIST (Continued)

CROSS REFERENCE INDEX LIST (Continued)

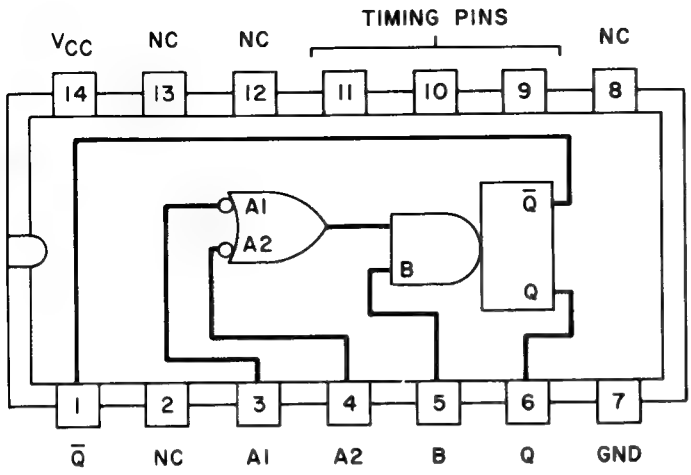
Panel, Control, Unit Signal Processor	353D273	FO-76
Panel, MTI Sector Select, Unit 26	354D002	FO-20
Panel, Power Distribution	362D610	FO-114
Panel, Readout, Height	343D902	FO-73
Peak Selector P.C. Card	352D975	FO-82
Power Distribution Panel	362D610	FO-114
Power Distribution Unit, Auxiliary, Unit 31	353D379	FO-34
Power Supply, Communication, Unit 28	121B468	FO-104
Power Supply, IFF Unit 42	121B459	FO-103
Power Supply, U.S.P., No. 1, Unit 24	121B426	FO-101
Power Supply, U.S.P., No. 2, Unit 25	121B471	FO-102
Power Supply, -130VDC	128C472H94	FO-37
Range Azimuth Gating (RAG) Planar Array	352D870	FO-70
Readout, Digital Height (DHRO) Planar Array	352D872	FO-72
Readout Panel, Height	343D902	FO-73
Receiver Control Planar Array/Unit 10 Receiver Interconnection Diagram	352D871	FO-84
Receiver, IF, Height, P.C. Card	352D969	FO-74
Receiver, IF, Search/MTI, P.C. Card	356D394	FO-75
Receiver, JATS/Weather, P.C. Card	352D984	FO-77
Receiver Matrix	338D033	FO-51
Receiver, Unit 10, Interconnection Diagram/ Receiver Control Planar Array	352D871	FO-84
Regulator, +5V or -5.2V, P.C. Card	25137(FIC 09004)	FO-105
Regulator, +6V or -6V, P.C. Card	25143(FIC 09004)	FO-106
Regulator, +12V or -12V, P.C. Card	25146(FIC 09004)	FO-107
Regulator, +28V/+25V, P.C. Card	25134(FIC 09004)	FO-108
Regulator, -50V, P.C. Card	25140(FIC 09004)	FO-109
RF Amplifier	345D787	FO-49
Ring-Out, Tropo, P.C. Card	355D064	FO-93
Ring-Out, 20 Hz, P.C. Card	355D071	FO-94
Search/MTI IF Receiver P.C. Card	356D394	FO-75
Sector Select Panel, MTI, Unit 26	354D002	FO-20
Selector, Beam Pair, P.C. Card	352D937	FO-80
Selector, Peak, P.C. Card	352D975	FO-82
Sensor, Vertical	150B476	FO-38
Sidelobe Blanker P.C. Card	352D980	FO-83
Signal Generator	353D985	FO-39
Speaker Amplifier P.C. Card	355D059	FO-92
Squaring Circuit P.C. Card	352D889	FO-62
STALO Reference, Switched	572F445	FO-40
STC Generator/COHO Splitter, P.C. Card	352D986	FO-79
Subtractor, Beam, P.C. Card	352D973	FO-81

CROSS REFERENCE INDEX LIST (Continued)

CROSS REFERENCE INDEX LIST (Continued)

371 MHz	Band Pass Filter	FO-43
371 MHz	Power Amplifier	FO-44
121B426	U.S.P. Power Supply No. 1, Unit 24	FO-101
121B471	U.S.P. Power Supply No. 2, Unit 25	FO-102
121B459	IFF Power Supply, Unit 42	FO-103
121B468	Communication Power Supply, Unit 28	FO-104
150B476	Vertical Sensor	FO-38
150B425	Amplifier - Demodulator	FO-53
25134 (FIC 09004)	+25V/+28V Regulator P.C. Card	FO-108
25137 (FIC 09004)	+5V or -5.2V Regulator P.C. Card	FO-105
25140 (FIC 09004)	-50V Regulator P.C. Card	FO-109
25143 (FIC 09004)	+6V or -6V Regulator P.C. Card	FO-106
25146 (FIC 09004)	+12V or -12V Regulator P.C. Card	FO-107
128C472H94	-130VDC Power Supply	FO-37
332D900	Microwave Switch Driver	FO-48
338D033	Receiver Matrix	FO-51
338D942	IFF Switch Driver P.C. Card	FO-96
324D839	Air Conditioner Control Unit, Unit 36	FO-34/ 35E9-118-3
343D834	X6 Multiplier	FO-42
343D837	371 MHz Band Pass Filter	FO-43
343D858	First Frequency Doubler	FO-45
343D865	X4 Frequency Multiplier	FO-46
343D902	Height Readout Panel	FO-73
343D931	60 MHz Oscillator and Oscillator Gate	FO-41
345D036	Control Monitor, Unit 40	FO-95
345D689	371 MHz Power Amplifier	FO-44
345D787	RF Amplifier	FO-49
353D273	Unit Signal Processor Control Panel	FO-76
351D939	Illumination Dimmer Box, Unit 32	FO-34
352D856	Canceller/Decoder Planar Array	FO-85
352D857	Dual Integrator Planar Array	FO-66
352D858	Channel Control Planar Array	FO-65
352D859	Synchronizer No. 1 Planar Array	FO-63
352D860	Synchronizer No. 2 Planar Array	FO-64
352D861	BITE Planar Array	FO-59
352D862	Height Computer No. 1 Planar Array	FO-55
352D863	Height Computer No. 2 Planar Array	FO-56
352D865	Height Evaluator Planar Array	FO-57
352D867	Evaluator Memory Planar Array	FO-58
352D868	JATS Planar Array	FO-61
352D870	Range Azimuth Gating (RAG) Planar Array	FO-70
352D871	Unit 10, Receiver, Interconnection Diagram/Receiver Control Planar Array	FO-84
352D872	Digital Height Readout (DHRO) Planar Array	FO-72
352D877	A/D Converter P.C. Card	FO-54
352D879	8-Bit Memory P.C. Card	FO-67

CROSS REFERENCE INDEX LIST (Continued)



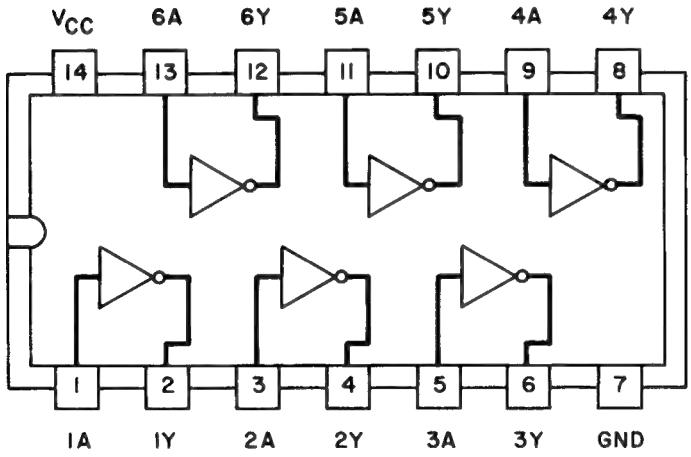
NOTE:
NC = NO CONNECTION

TRUTH TABLE

Tn INPUT			Tn+1 INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	0	1	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

4414A-BF-101A

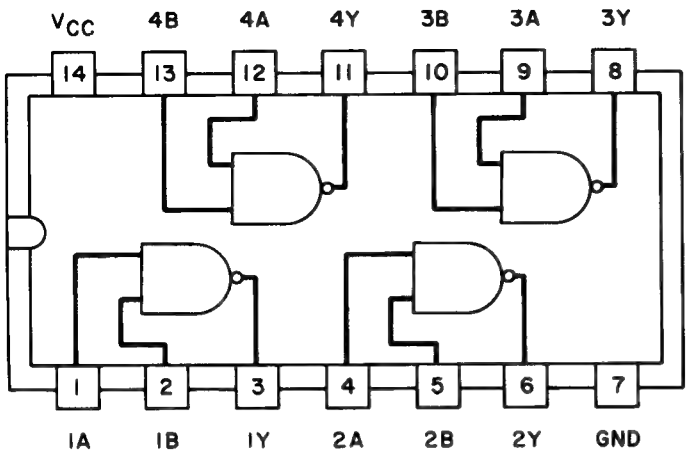
Figure 1. Monostable Multivibrator (128C823H12)



NOTE:
POSITIVE LOGIC:
$Y = \overline{A}$

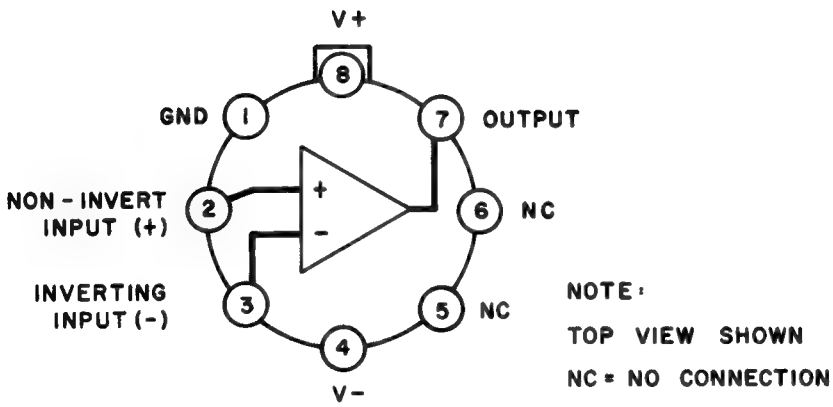
4414A-BF-102A

Figure 2. Hex Inverter (128C821H04, 578R558H02, 578R560H02)



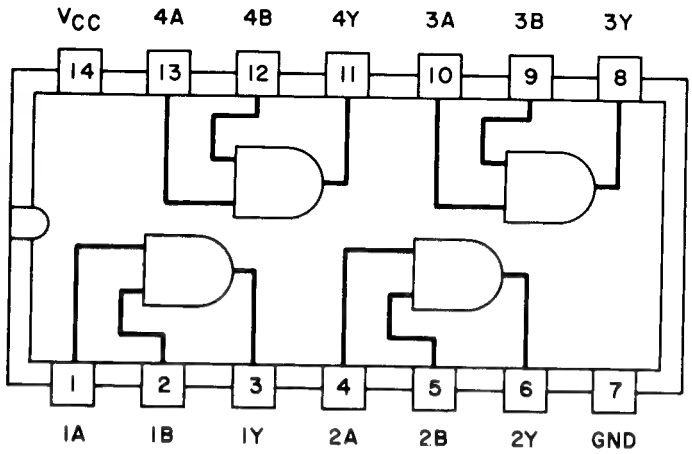
4414A-BF-103A

Figure 3. Quad 2-Input Positive NAND Gate (128C821H01, 578R553H02, 581R135H01, 582R722H01, M38510/00302BCB)



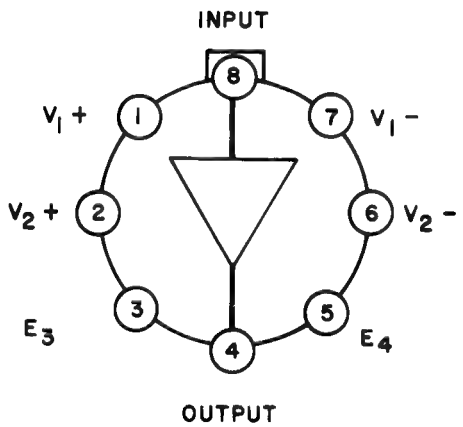
4414A-BF-104A

Figure 4. Differential Comparator (128C213H01, 581R500H84)



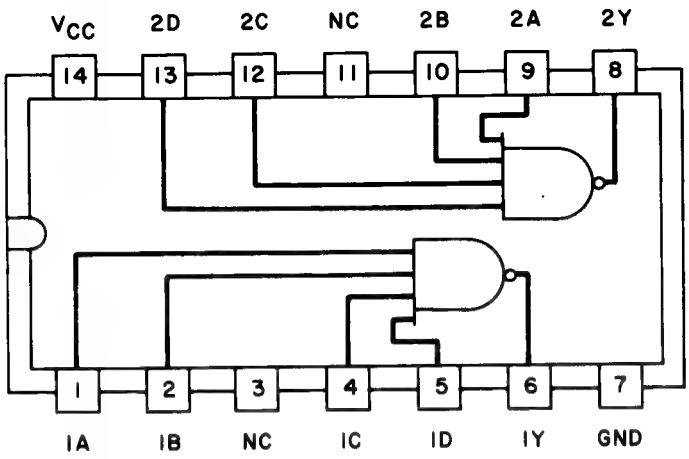
4414A-BF-105A

Figure 5. Quad 2-Input AND Gate (578R988H01)



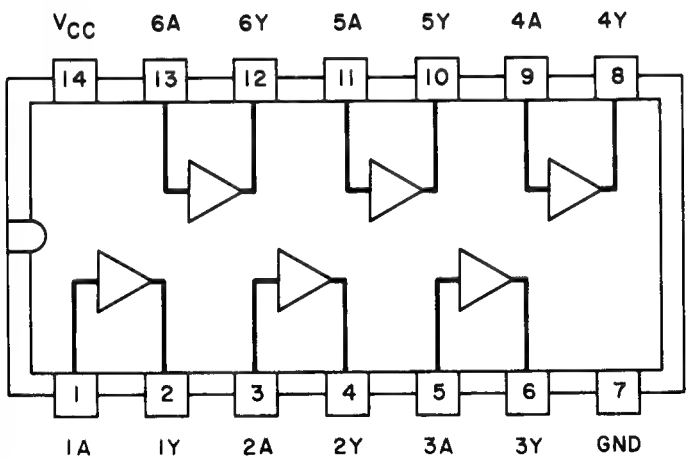
4414A-BF-106A

Figure 6. Analog Current Amplifier (649A819H01)



44I4A-BF-I07A

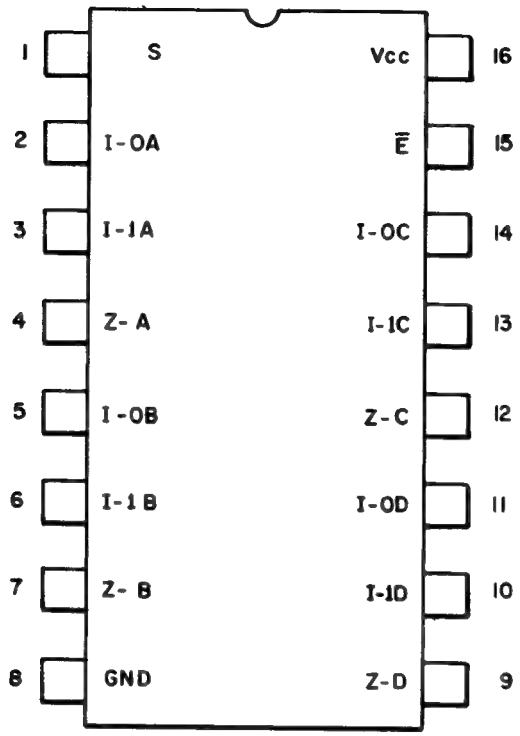
Figure 7. Dual 4-Input NAND Gate (578R562H02, 128C821H07, 581R548H02)



44I4A-BF-I08A

Figure 8. Hex Buffer/Driver (581R500J44)

CONNECTION DIAGRAMS
DIP (TOP VIEW)



TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Logic Level

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Figure 9. Quad 2-Input Multiplexer (649A815H02) (Sheet 1 of 2)

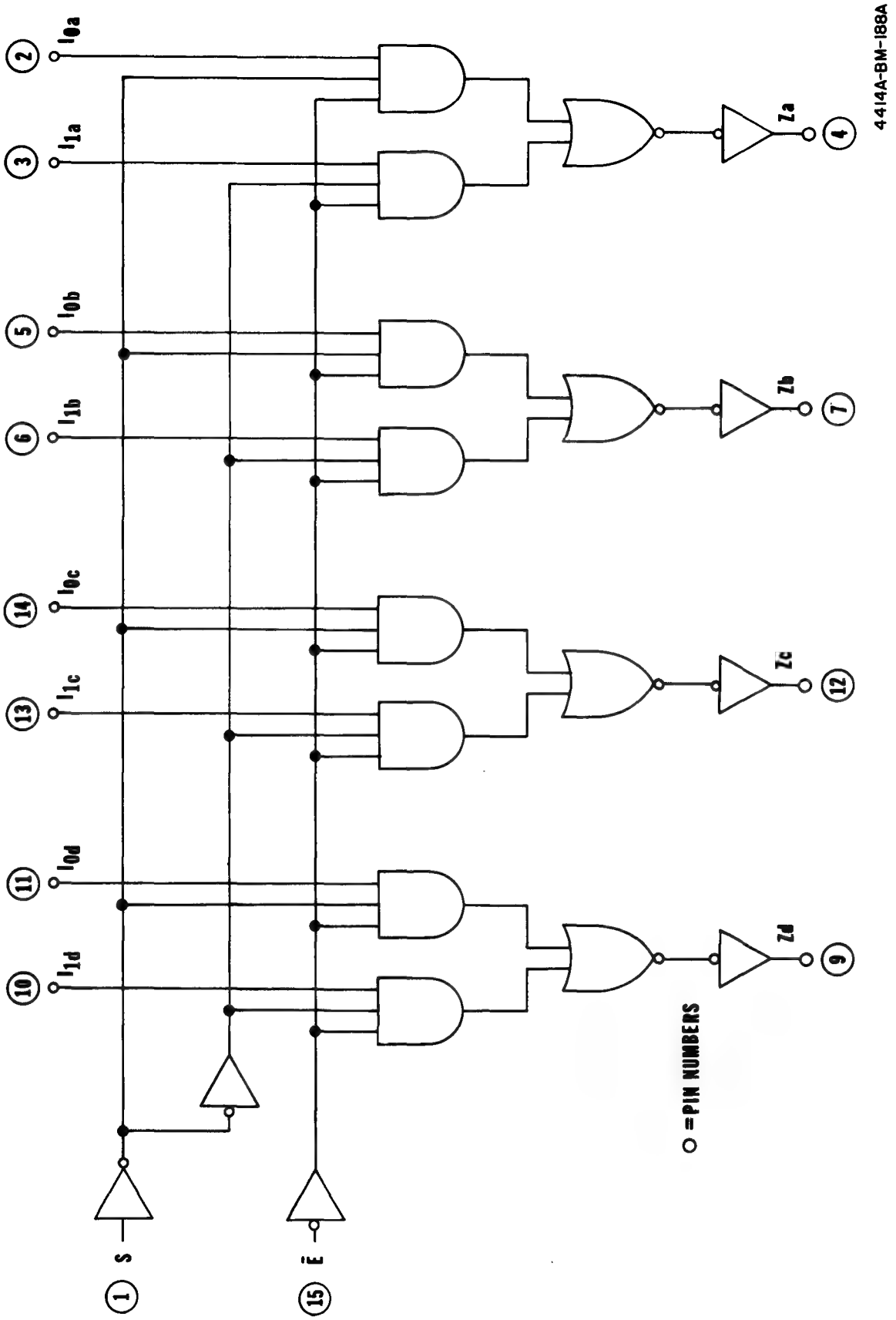
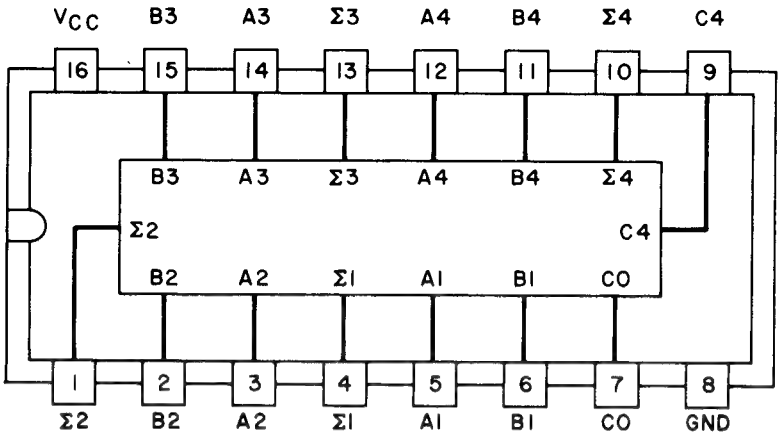


Figure 9. Quad 2-Input Multiplexer (649A815H02) (Sheet 2 of 2)



NOTE: POSITIVE LOGIC

FUNCTION TABLE

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

NOTE: Input conditions at A3, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

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Figure 10. 4-Bit Binary Full Adder (581R646H01) (Sheet 1 of 2)

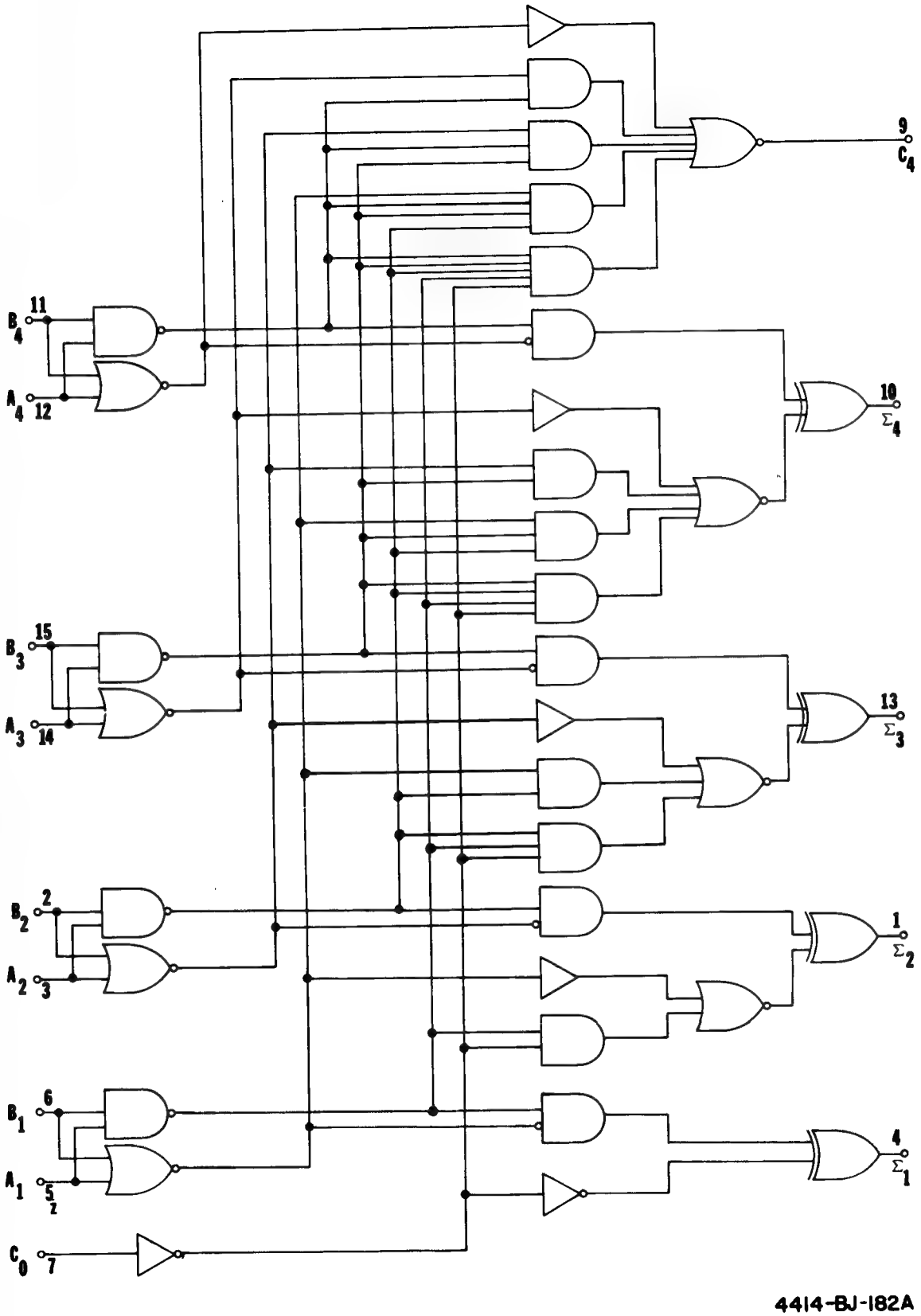
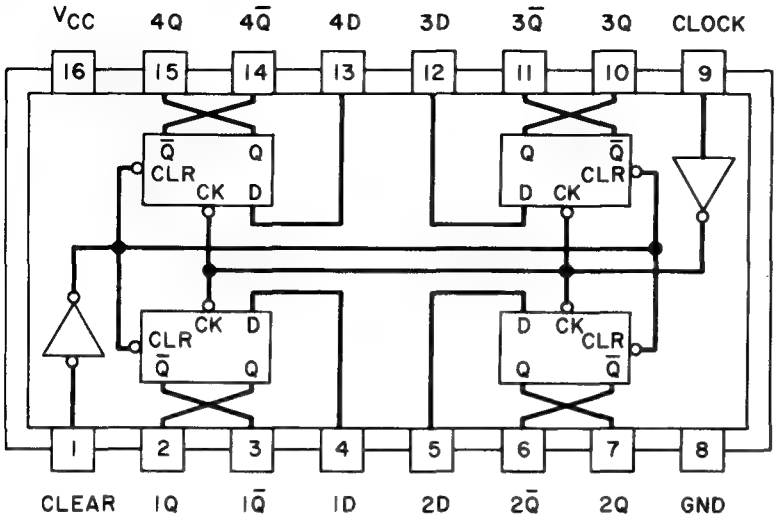


Figure 10. 4-Bit Binary Full Adder (581R646H01) (Sheet 2 of 2)



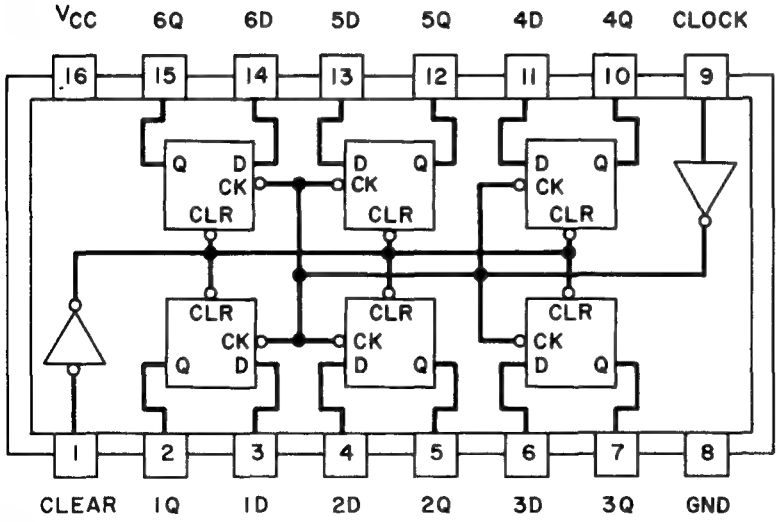
TRUTH TABLE

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established.

4414A-BF-111A

Figure 11. Quad D-Type Flip-Flop (578R995H01)

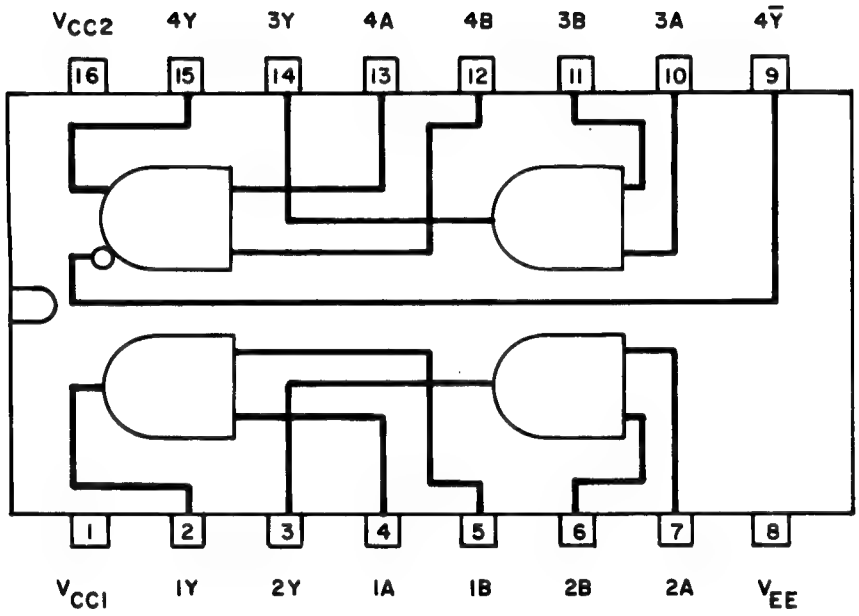


TRUTH TABLE

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

4414A-BF-112A

Figure 12. Hex D-Type Flip-FLop (578R995H02)



4414-BF-178A

Figure 13. Quad 2-Input AND Gate (581R688H08)

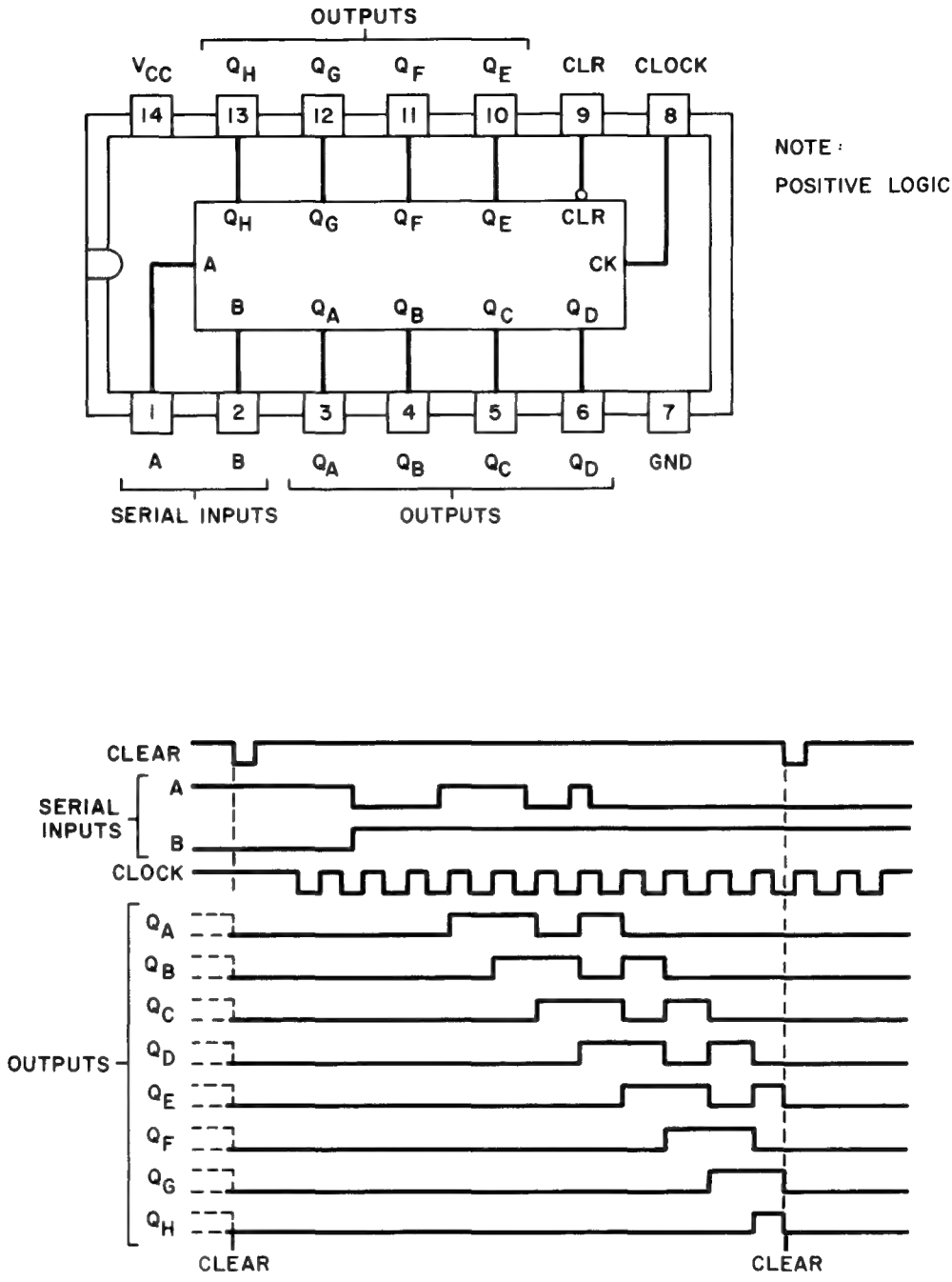


Figure 14. 8-Bit Serial-to-Parallel Shift Register (582R723H03) (Sheet 1 of 3)

FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state, L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent transition of the clock; indicates a one-bit shift.

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Figure 14. 8-Bit Serial-to-Parallel Shift Register (582R723H03) (Sheet 2 of 3)

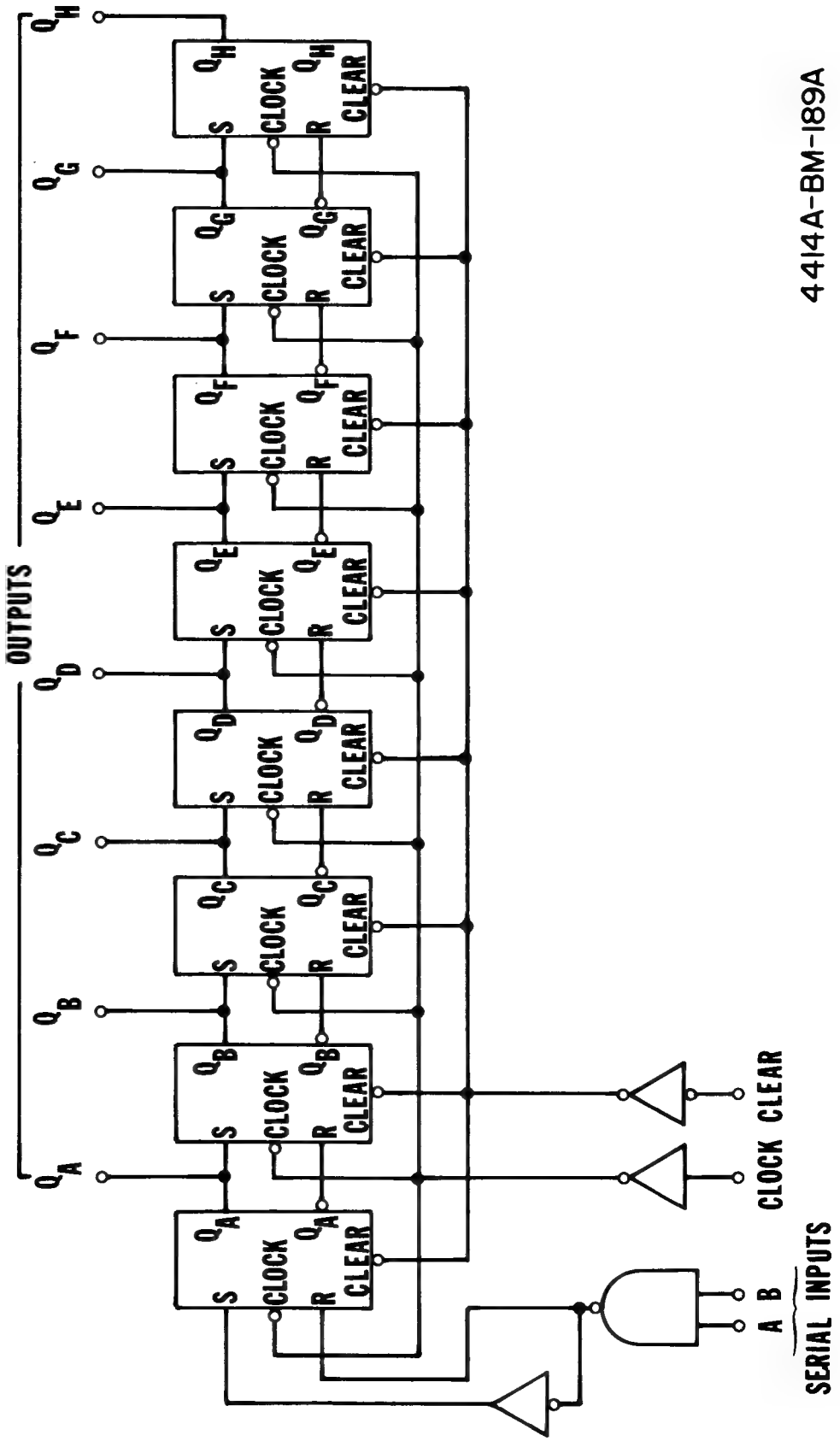
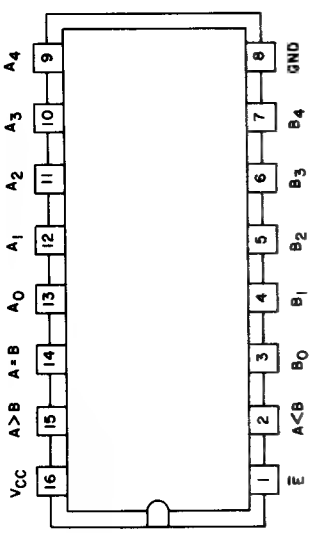


Figure 14. 8-Bit Serial-to-Parallel Shift Register (582R723H03)
(Sheet 3 of 3)

TRUTH TABLE

E	A_y	B_y	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A = Word B		L	L	H
L	Word A > Word B		L	H	L
L	Word B > Word A		H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage LEVEL



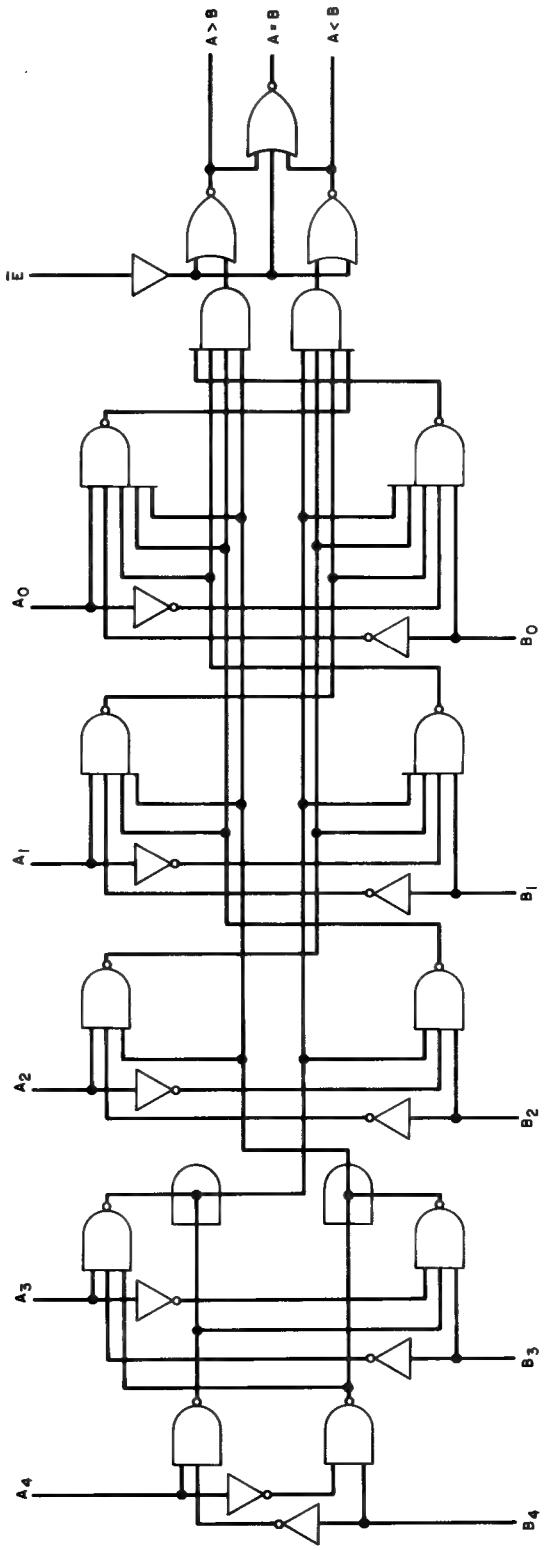
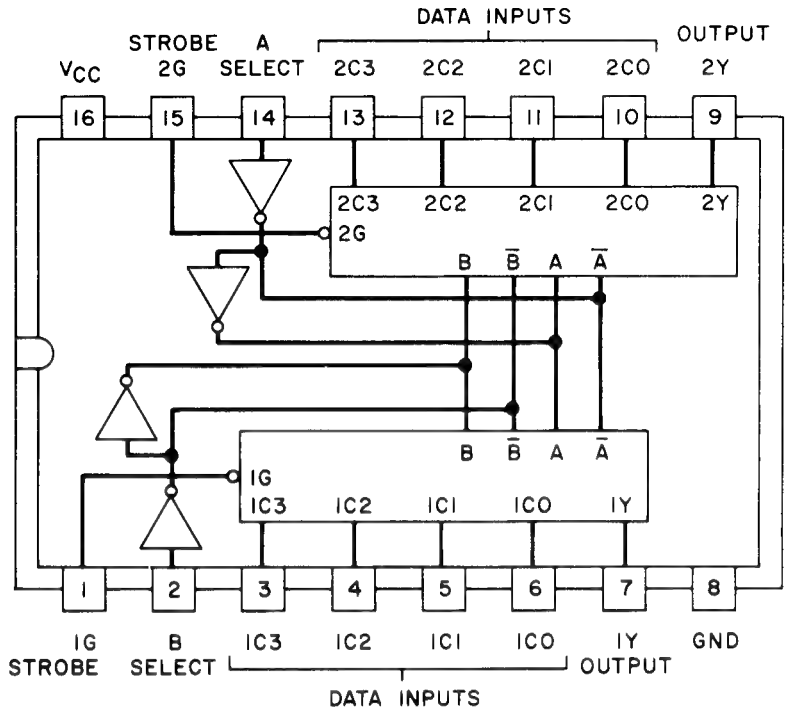


Figure 15. 5-Bit Comparator (649A818H02)



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

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Figure 16. Dual 4-Input Multiplexer (581R019H01) (Sheet 1 of 2)

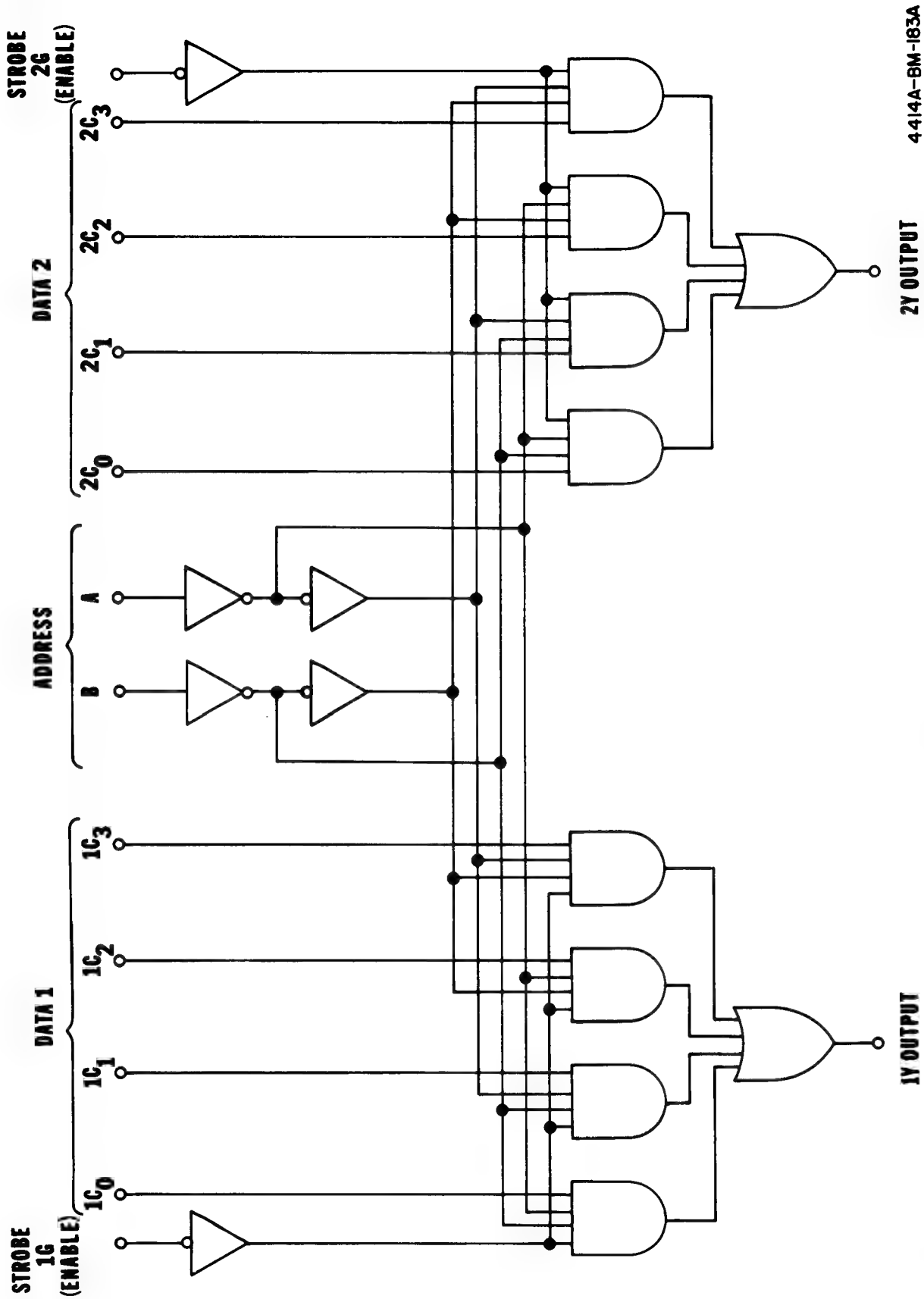

Figure 16. Dual 4-Input Multiplexer (581R019H01) (Sheet 2 of 2)

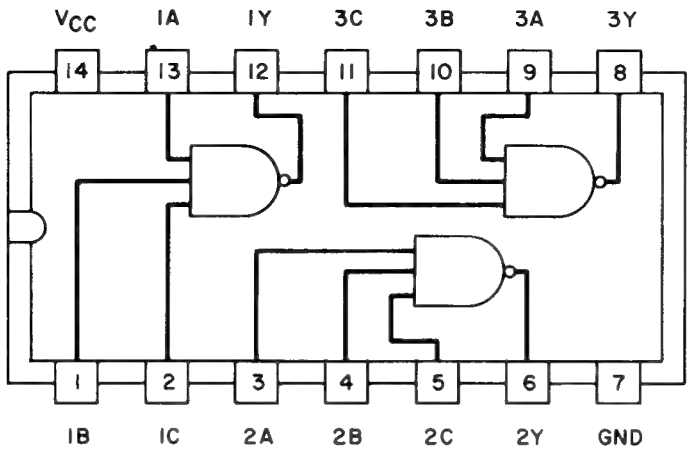

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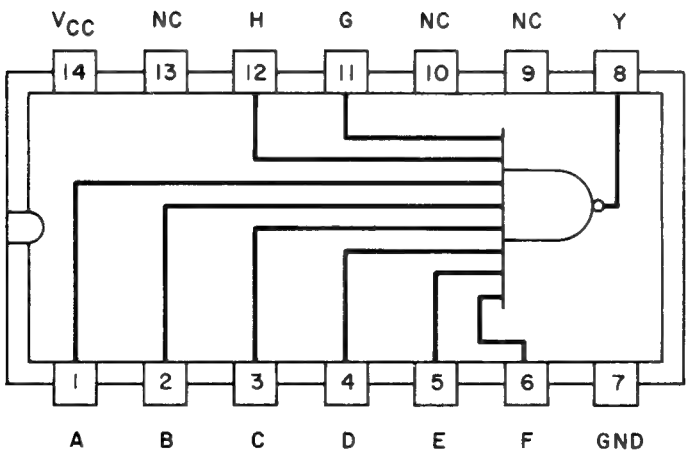
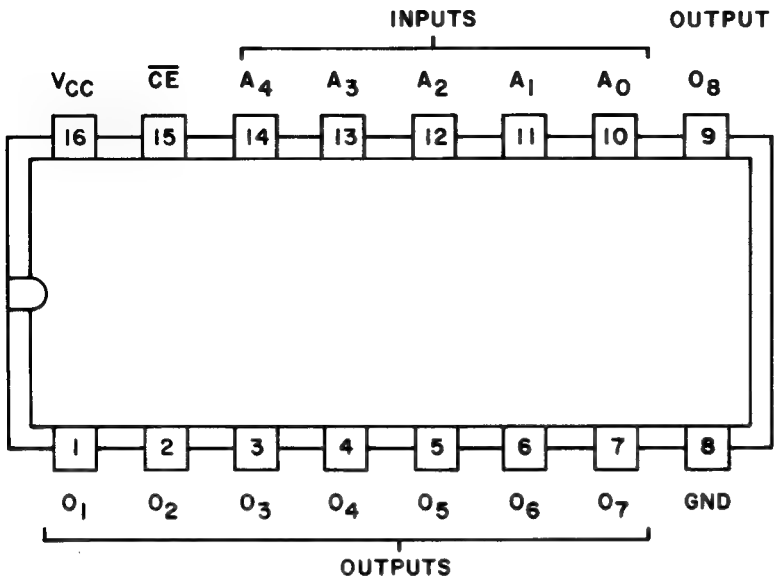
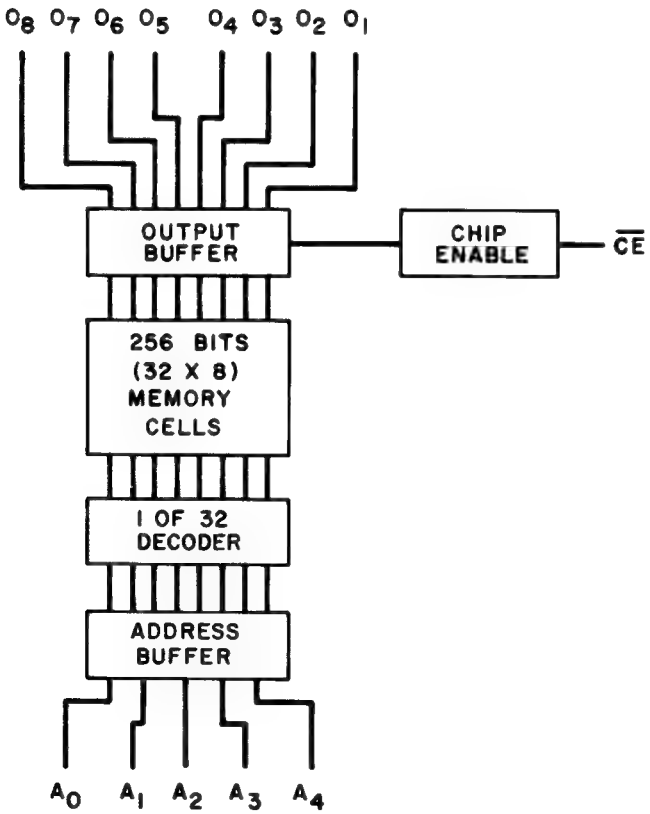
Figure 17. Triple 3-Input NAND Gate (581R500J26, 578R574H03 M38510/00103 BCB)



4414A-BF-118A

Figure 18. 8-Input NAND Gate (578R613H02)

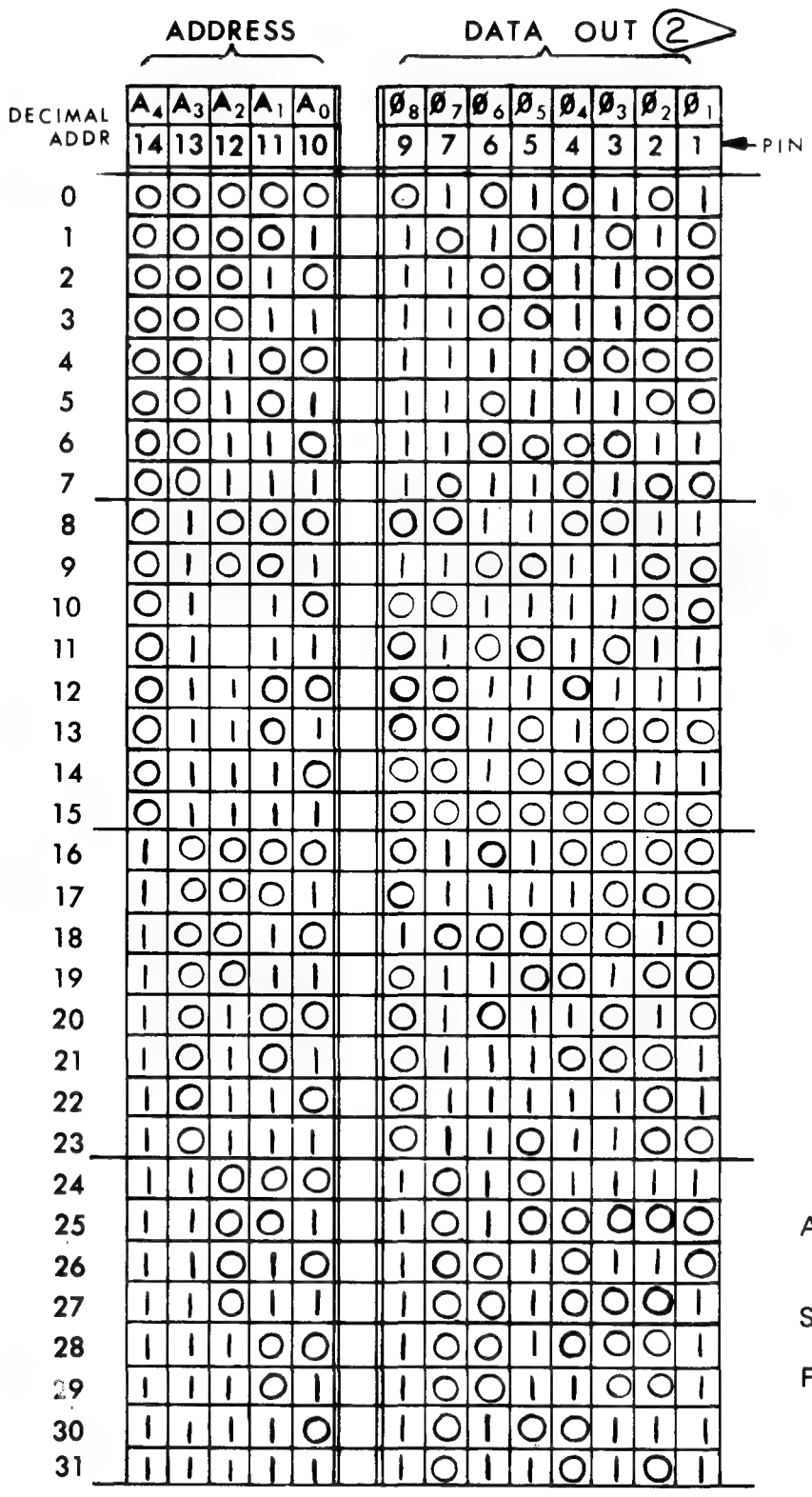




4414A-BM-197A

Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 1 of 9)

IM5610 – READ ONLY MEMORY PROGRAM



ARRAY–BITE
352D861

SLOT–U77

FUNCTION–HT. EVAL.
TEST WORDS

Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 2 of 9)

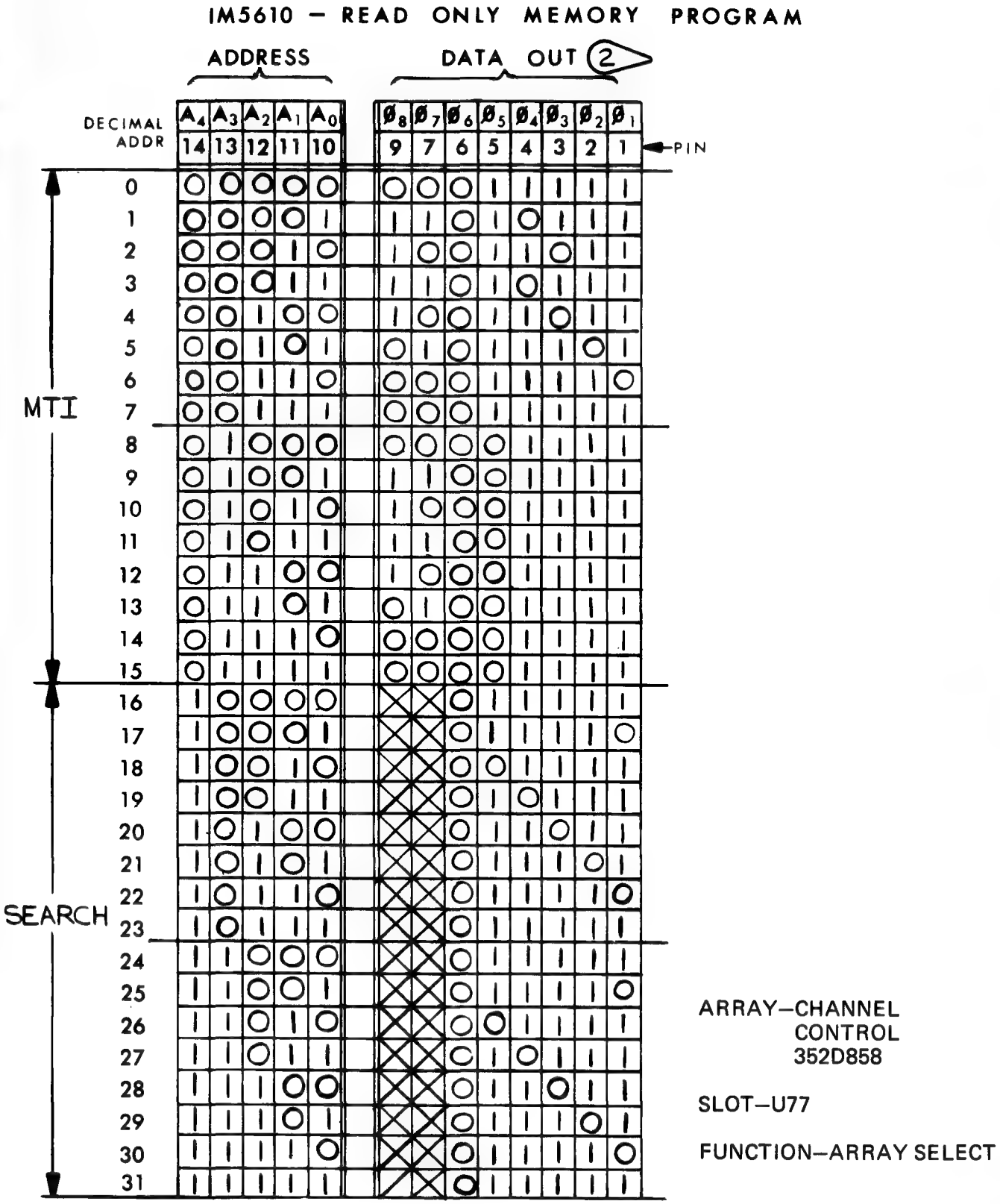


Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 3 of 9)

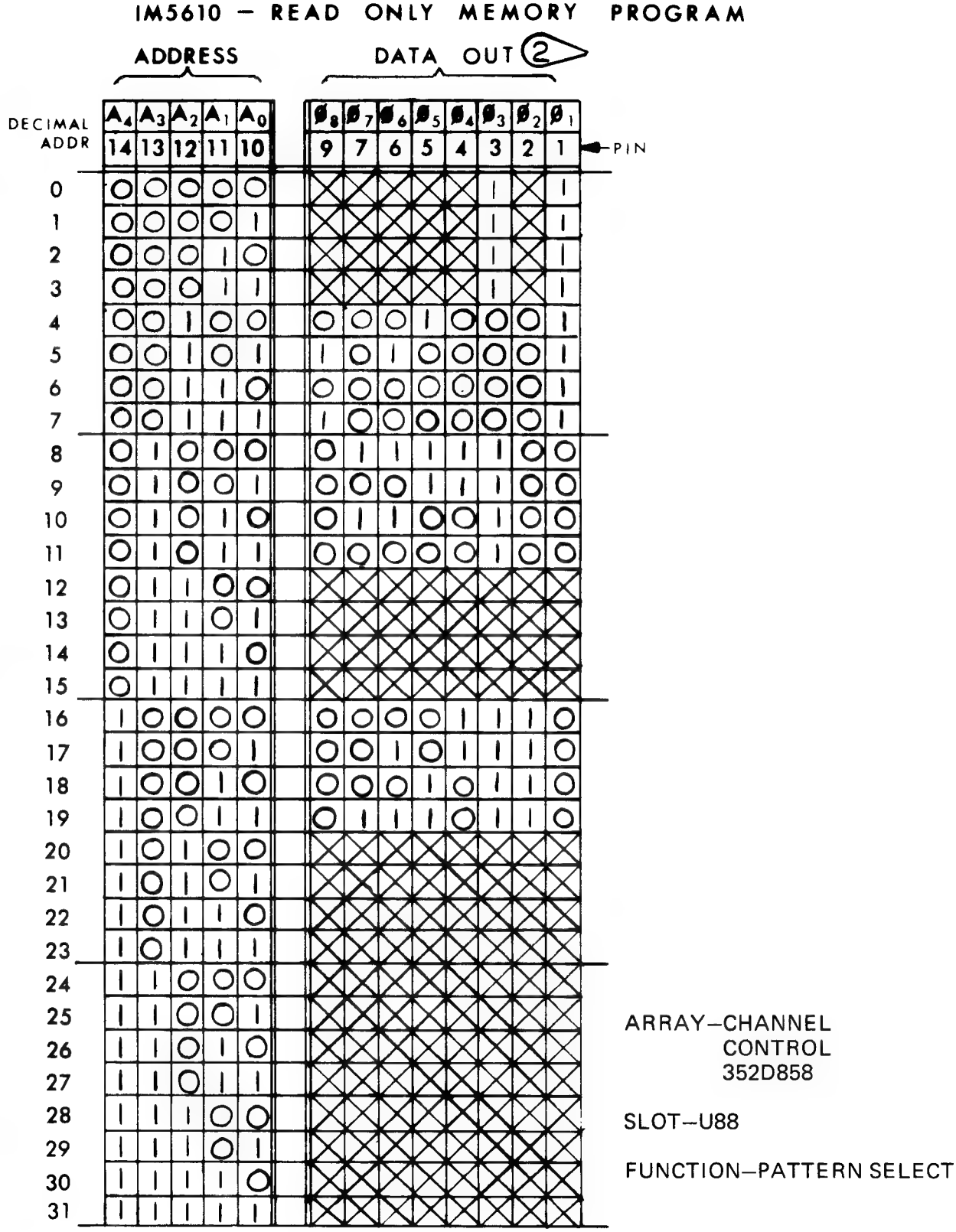
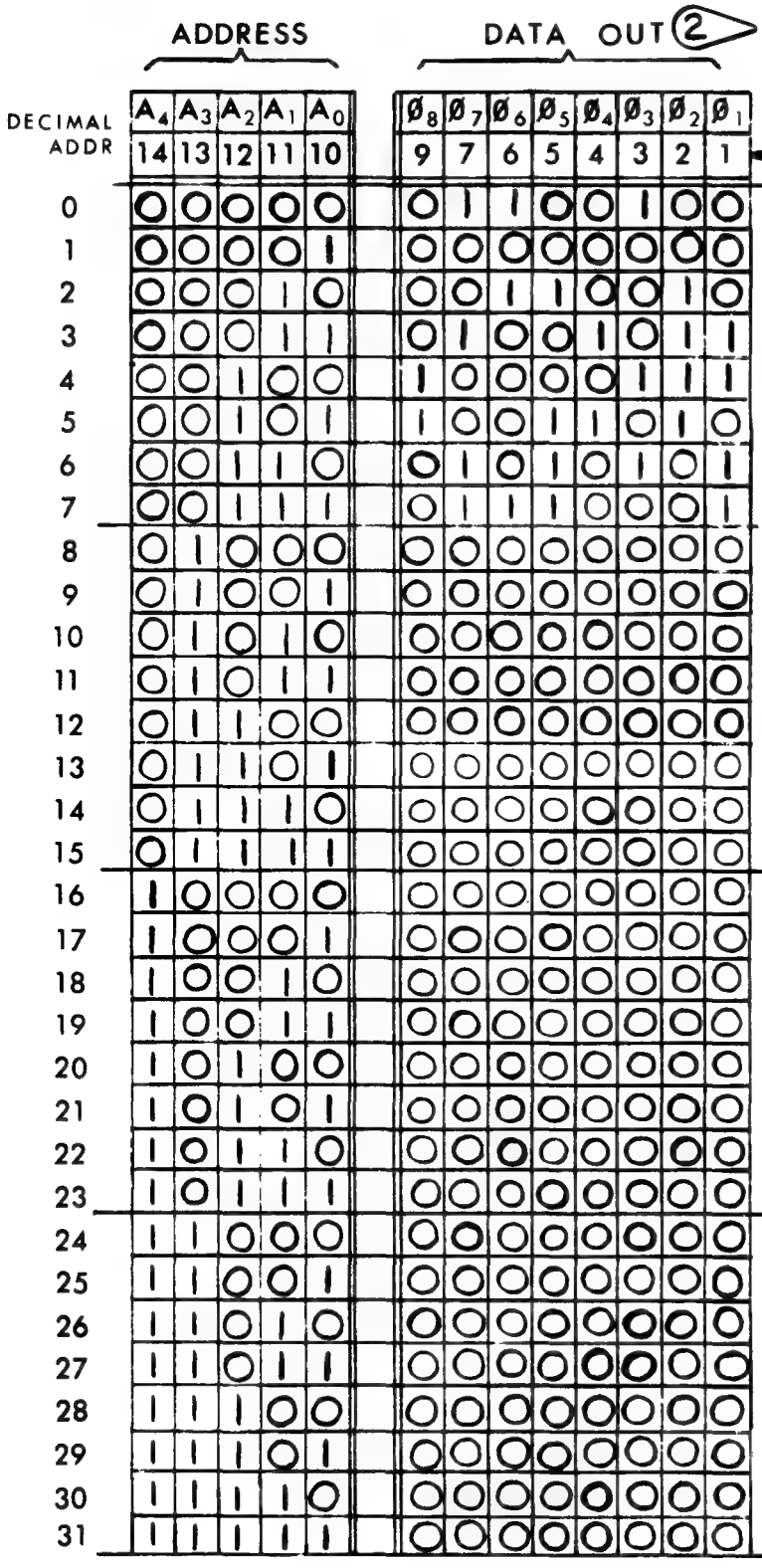


Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 4 of 9)

IM5610 – READ ONLY MEMORY PROGRAM



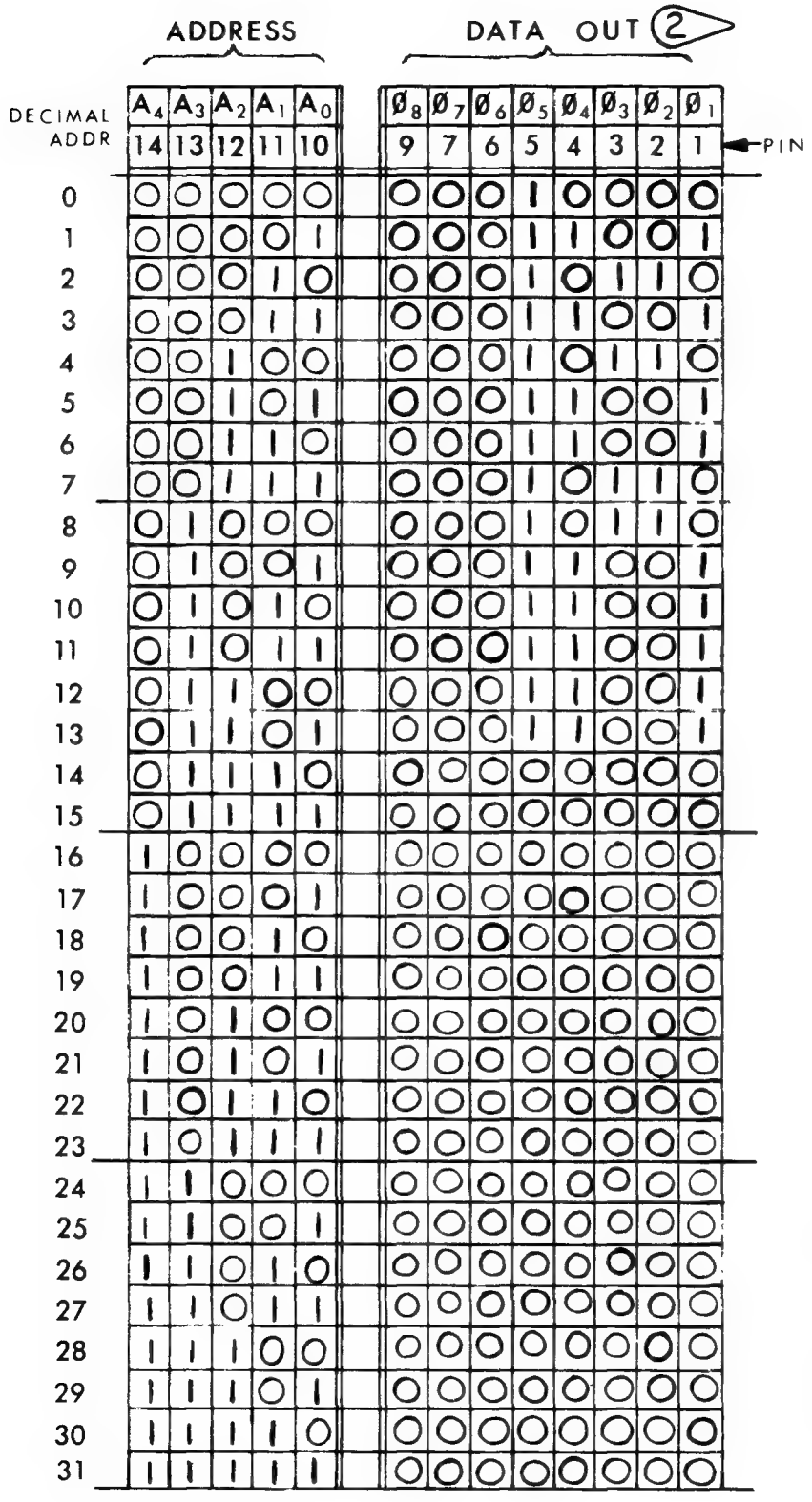
ARRAY–SYNCHRONIZER
NO. 1
352D859

SLOT–U04

FUNCTION–GEN. RNG. CNT.
COMPARES

Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 5 of 9)

IM5610 – READ ONLY MEMORY PROGRAM



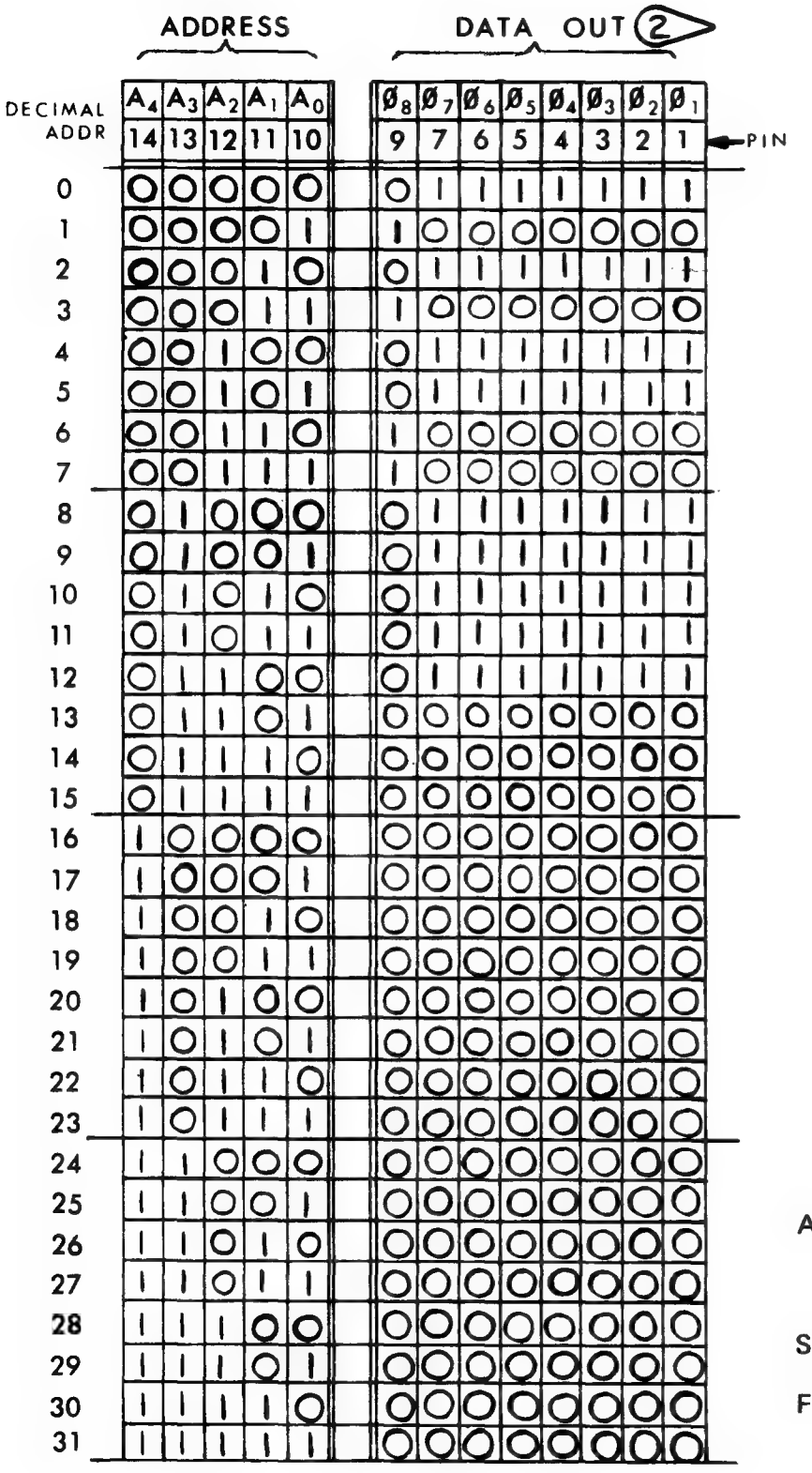
ARRAY–SYNCHRONIZER
NO. 2
352D860

SLOT–U72

FUNCTION–TEST WORD

Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 6 of 9)

IM5610 – READ ONLY MEMORY PROGRAM



ARRAY–CHANNEL CONTROL 352D858

SLOT–U93

FUNCTION–TEST WORD

Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 7 of 9)

IM5610 – READ ONLY MEMORY PROGRAM

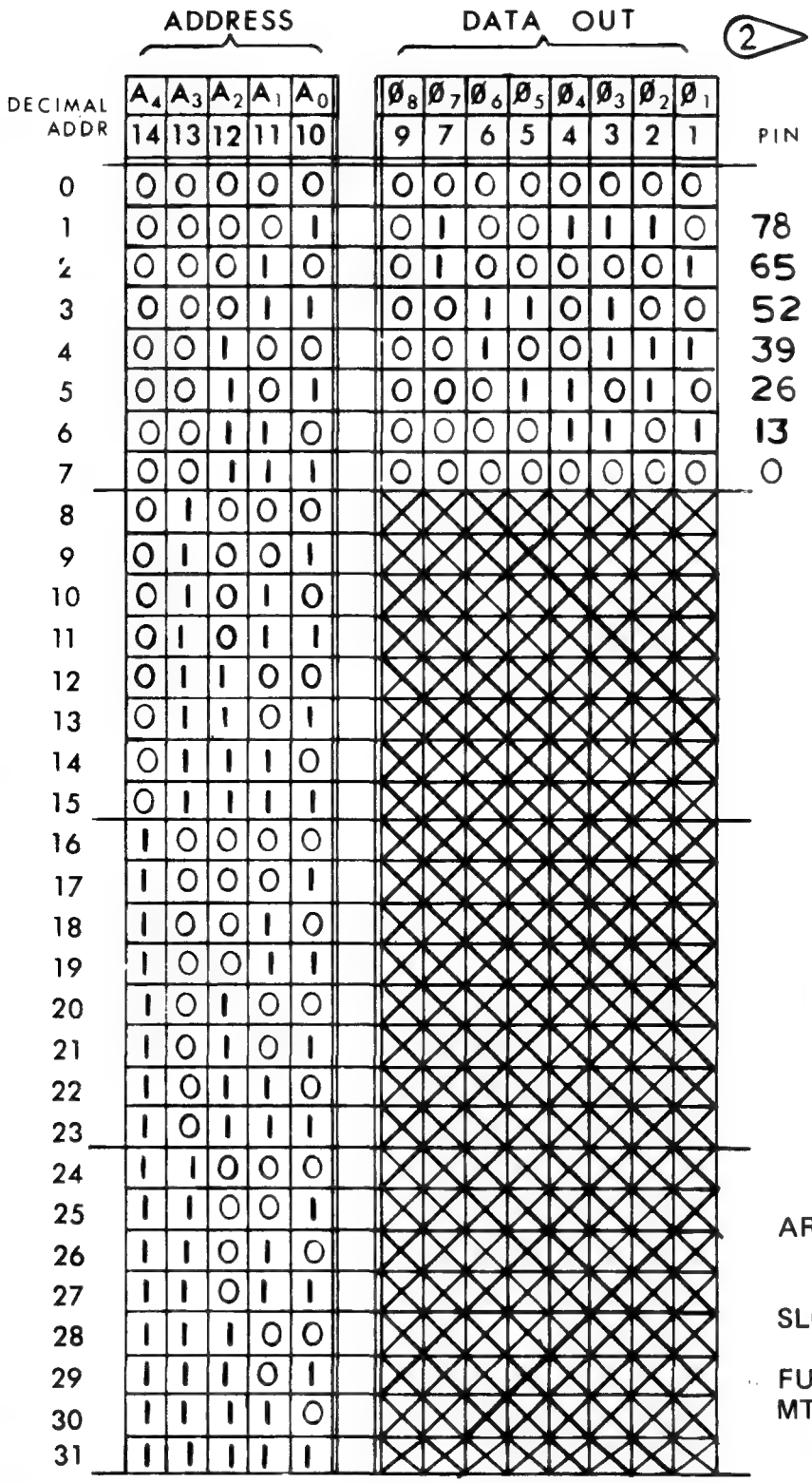
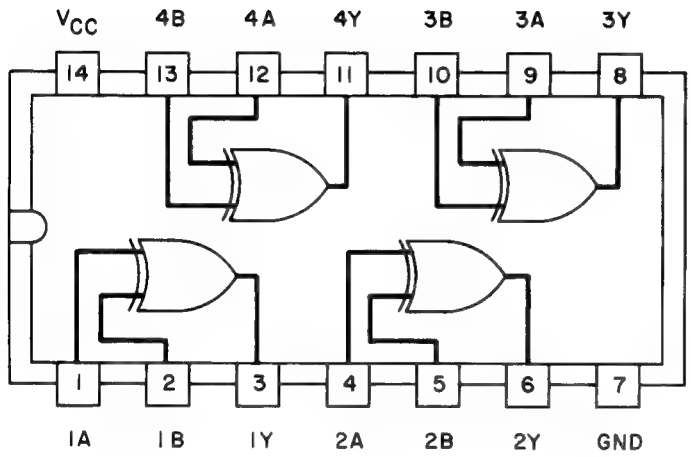


Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 8 of 9)

The 581R137H01 integrated circuit is a high-speed, electrically-programmable, fully-decoded TTL bipolar 256-bit read-only memory. It is organized as 32 words by 8 bits. Memory expansion is simple, three-state outputs. This device has on-chip address decoding and chip enable. The memory is fabricated with all logic level zeroes (low); logic level ones (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.

Figure 19. 256-BIT Bipolar PROM (581R137H01) (Sheet 9 of 9)



NOTE:
POSITIVE LOGIC:
$Y = A + B = \bar{A}B + A\bar{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

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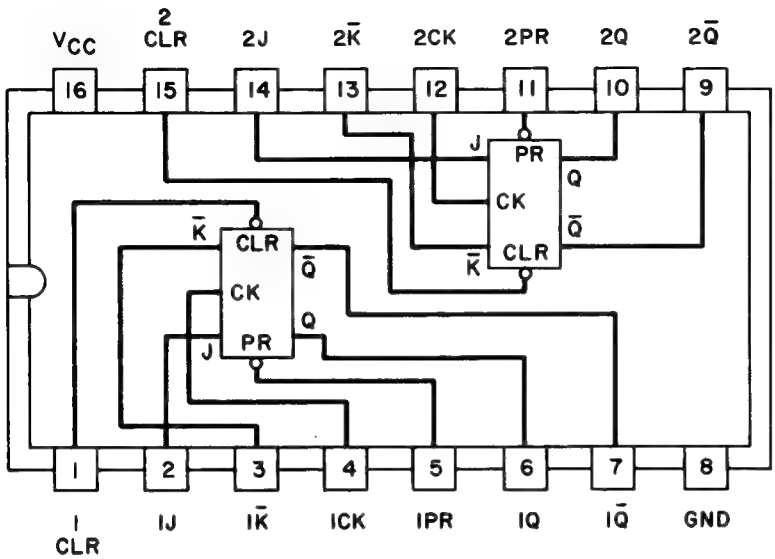
Figure 20. Quad 2-Input Exclusive OR Gate (M38510/00701BCB)



FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

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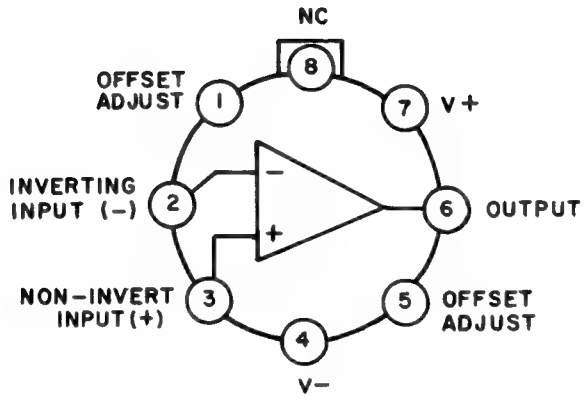
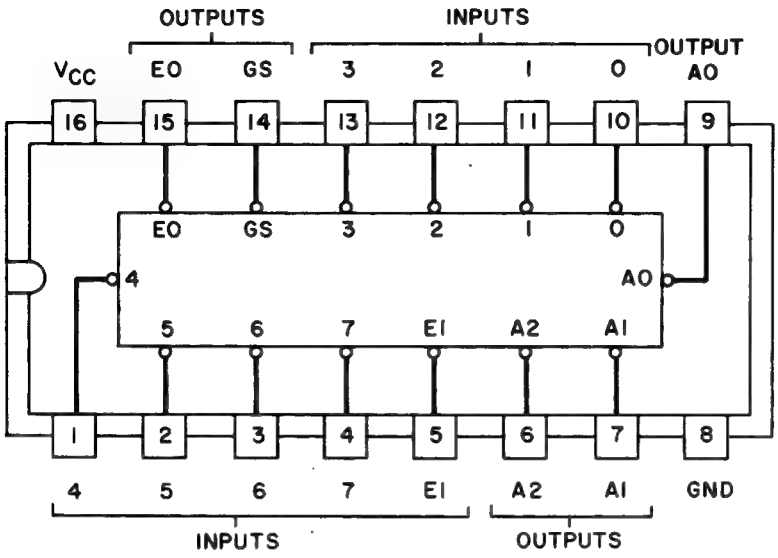
Figure 21. Dual J-K Positive Edge-Triggered Flip Flop (581R817H01)



NOTE: (1) TOP VIEW SHOWN
(2) PIN 4 CONNECTED TO CASE

4414A-BF-177A

Figure 22. Operational Amplifier (581R500J17, M38510/10101BGB)



FUNCTION TABLE

INPUTS									OUTPUTS				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

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Figure 23. 10-line Decimal-to-4-Line BCD Decoder (649A817H03) (Sheet 1 of 2)

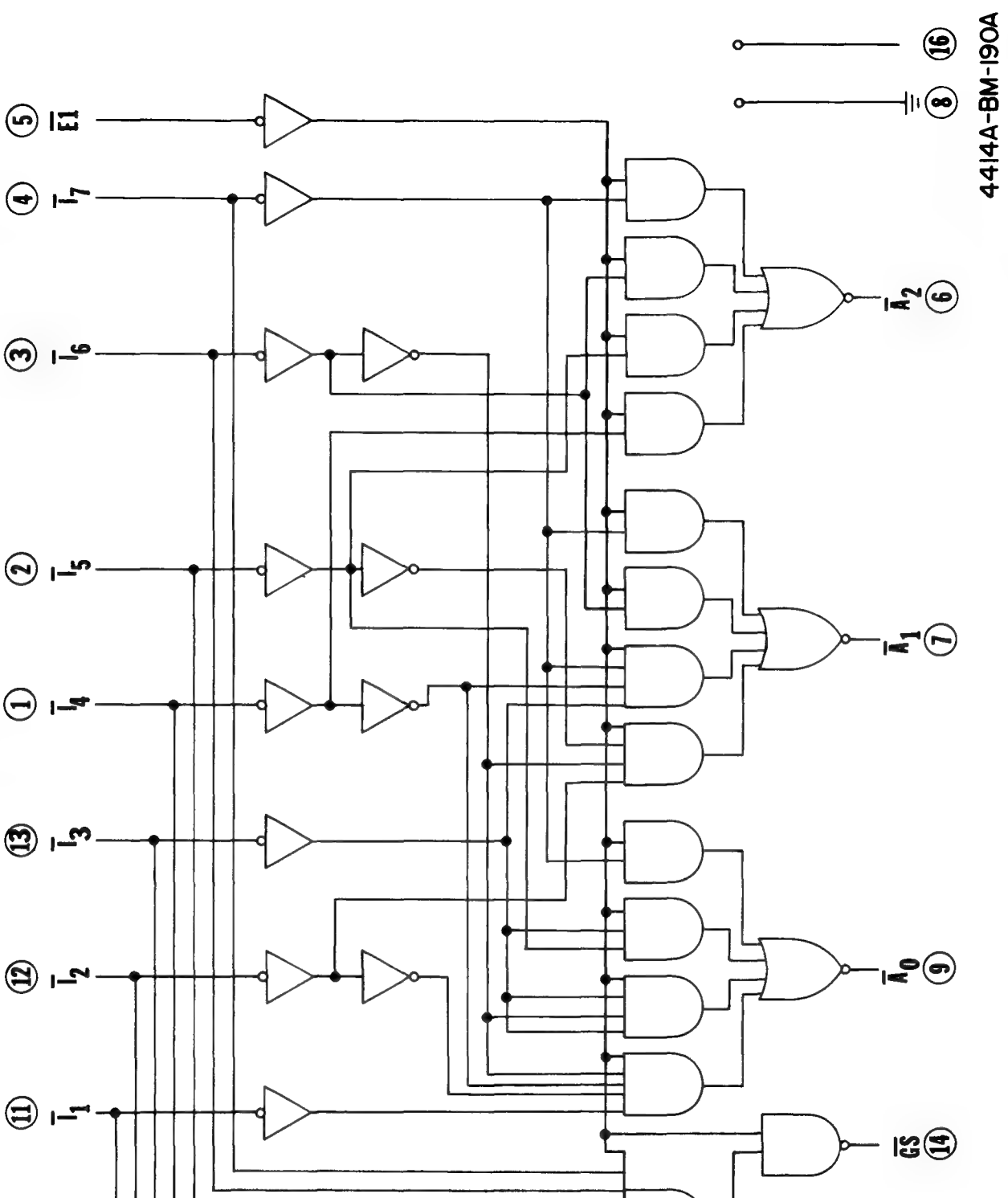
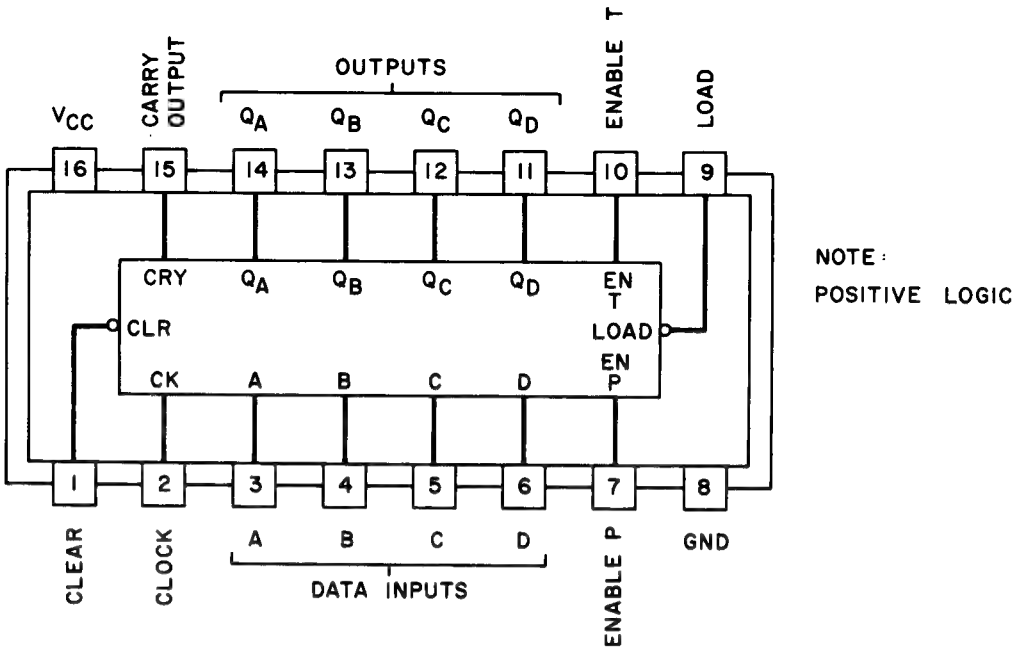


Figure 23. 10-line Decimal-to-4-Line BCD Decoder (649A817H03)
(Sheet 2 of 2)



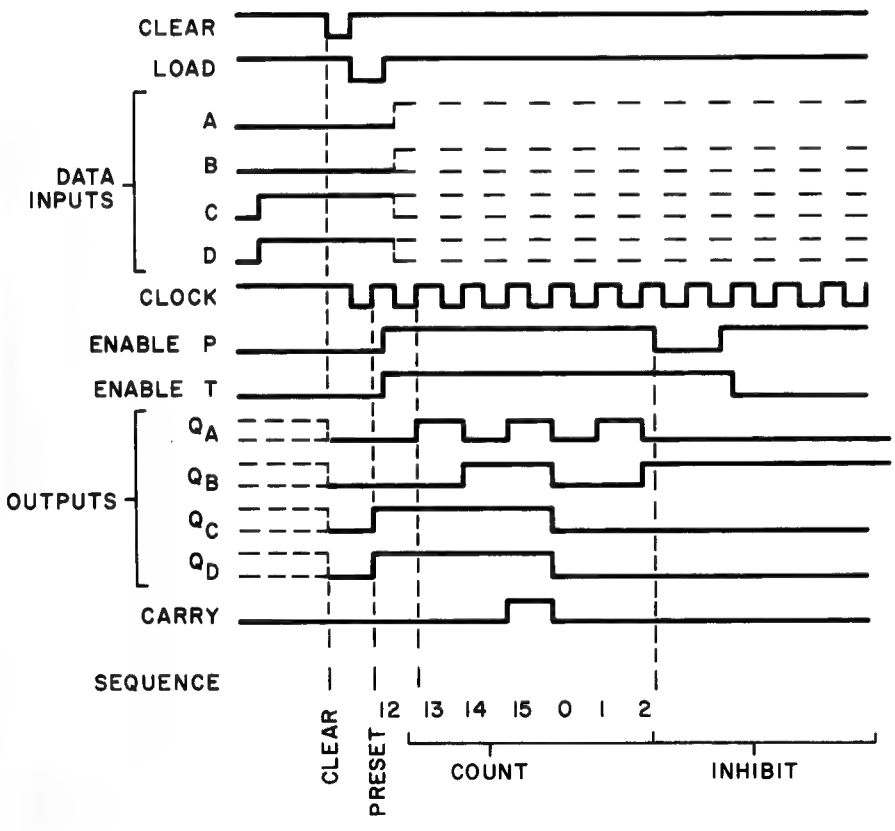


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Figure 24. Synchronous 4-Bit Binary Counter (581R500H36, 582R241H01) (Sheet 1 of 2)

MODE SELECTION

$\overline{PE}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

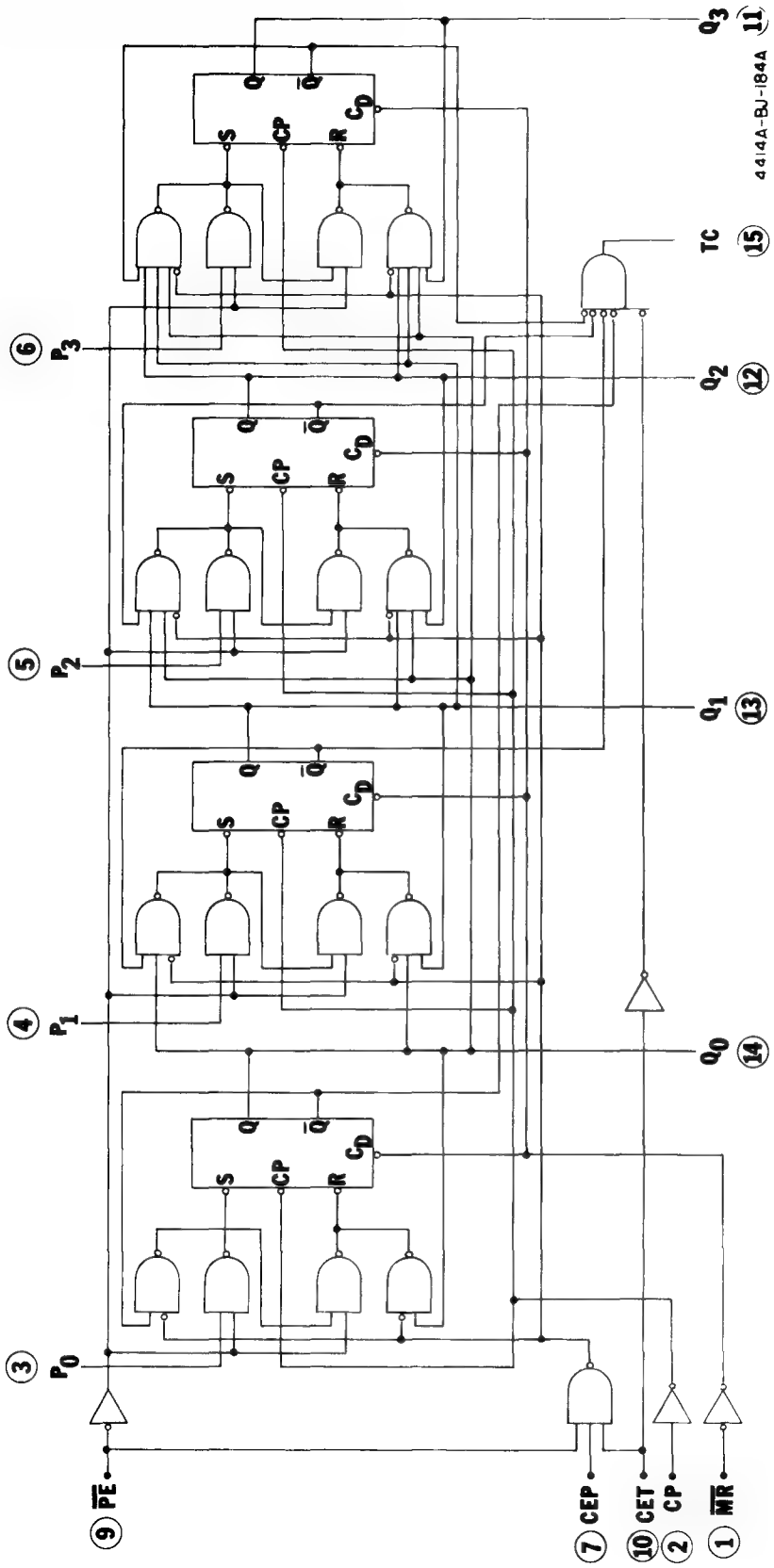
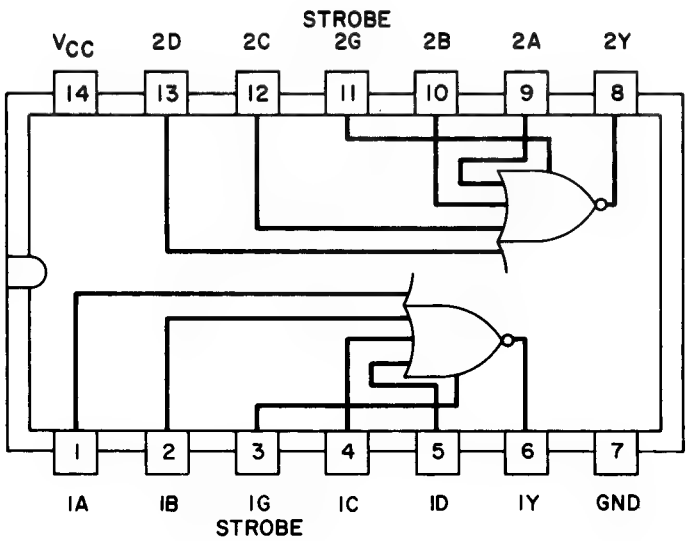


Figure 24. Synchronous 4-Bit Binary Counter (581R500H36, 582R241H01) (Sheet 2 of 2)

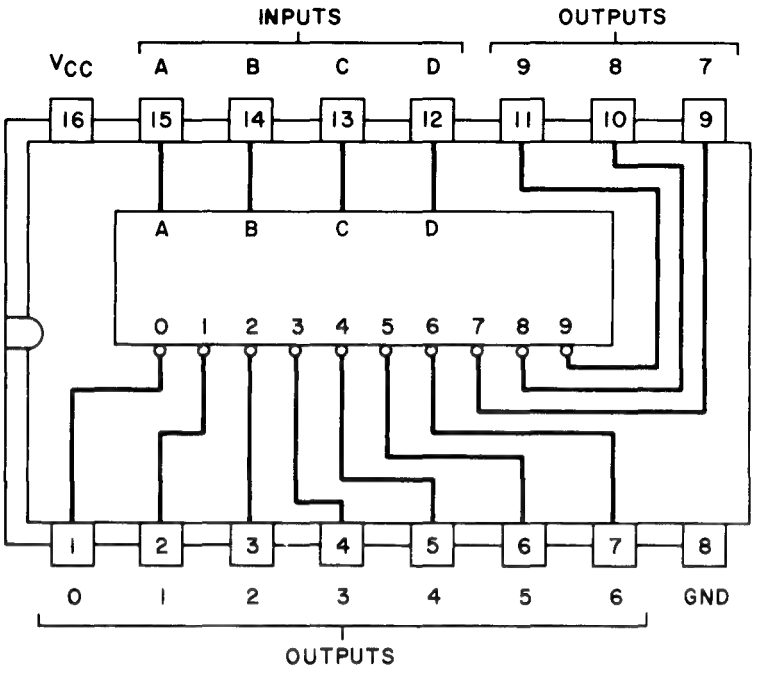


NOTE:

POSITIVE LOGIC, EACH GATE: $Y = \overline{G(A+B+C+D)}$

4414A-BF-125A

Figure 25. Dual 4-Input NOR Gate with Strobe (M38510/00403BCB)



FUNCTION TABLE

NO.	'42A,'L42 BCD INPUT				'43A,'L43 EXCESS-3-INPUT				'44A,'L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

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Figure 26. BCD-to-Decimal Decoder (M38510/01001BEB) (Sheet 1 of 2)

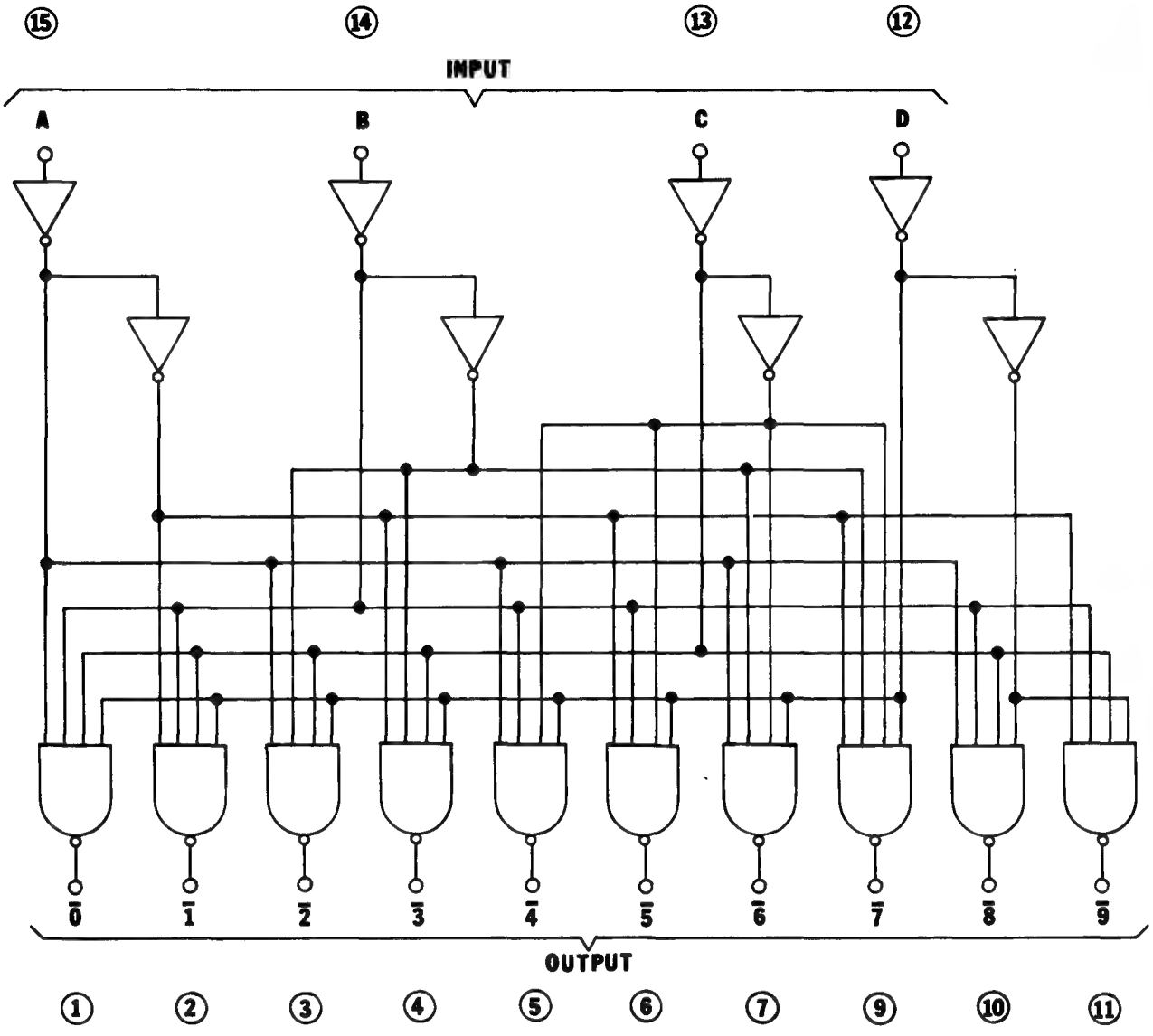
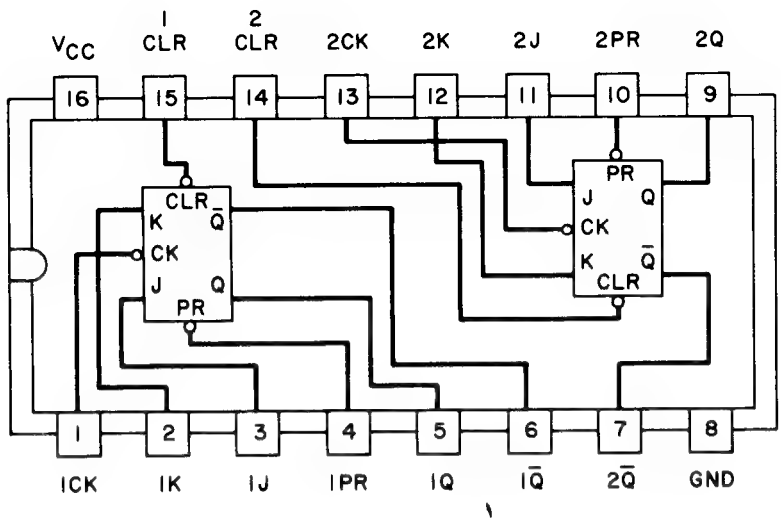


Figure 26. BCD-to-Decimal Decoder (M38510/01001BEB) (Sheet 2 of 2)



FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

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Figure 27. Dual J-K Negative Edge-Triggered Flip-Flop (581R136H01)

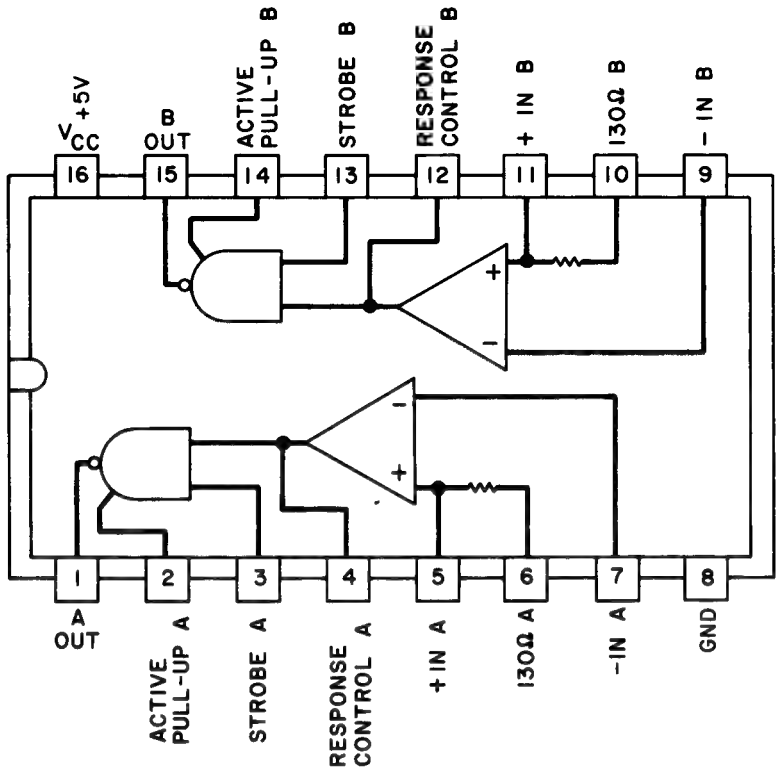


Figure 28. Dual Line Receiver (581R271H02)

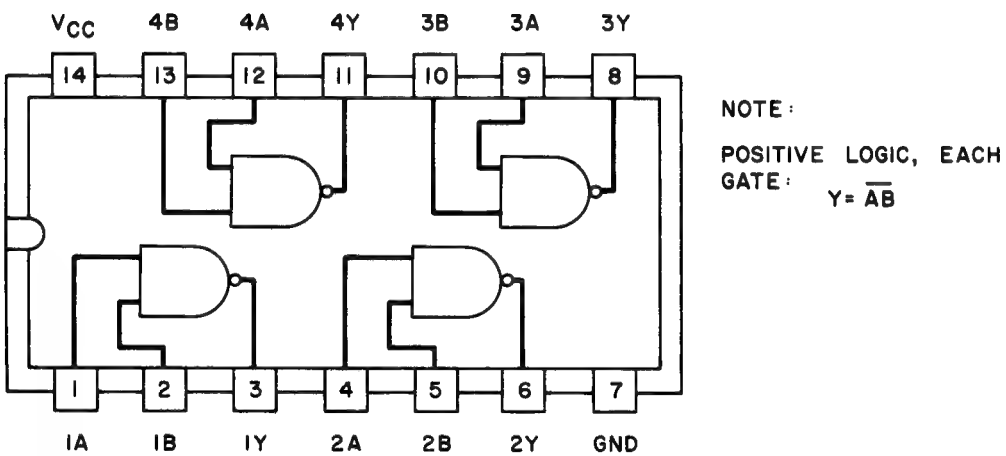
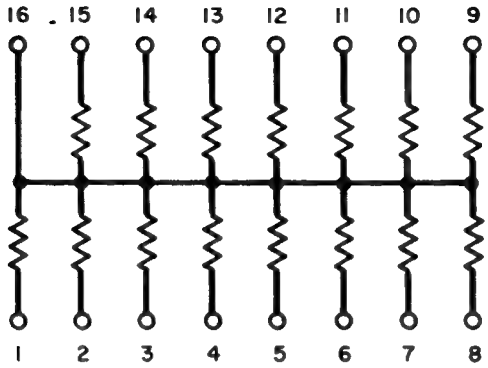


Figure 29. Quad 2-Input Positive NAND Gate (128C821H03, 578R559H02, M38510/00303BCB)



Note:

M8340102M102JB has 15 identical 1000 ±5% ohm resistors

M8340102M302JB has 15 identical 3000 ±5% ohm resistors

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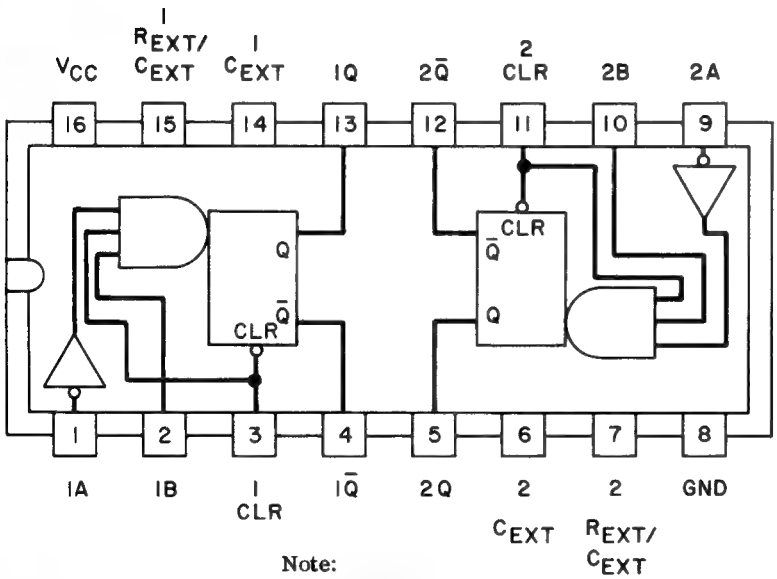
Figure 30. Resistor Network (M8340102)



FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

Note:

DC triggering from gated low level active (A) and high level active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended.

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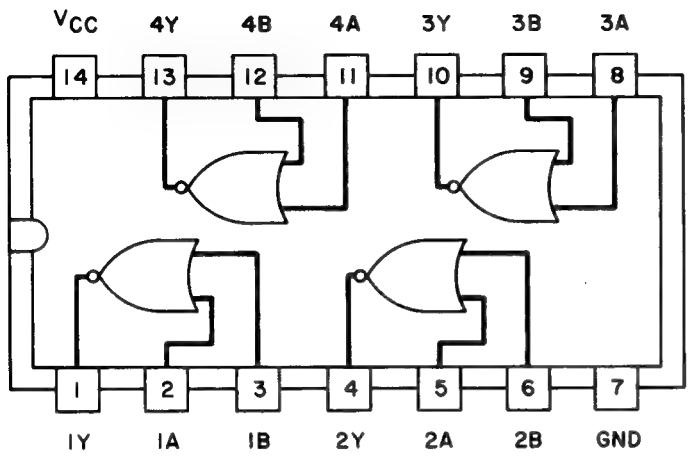
Figure 31. Dual Monostable Multivibrator (581R500H89)



NOTE:

POSITIVE LOGIC, EACH GATE: $Y = \overline{A + B}$

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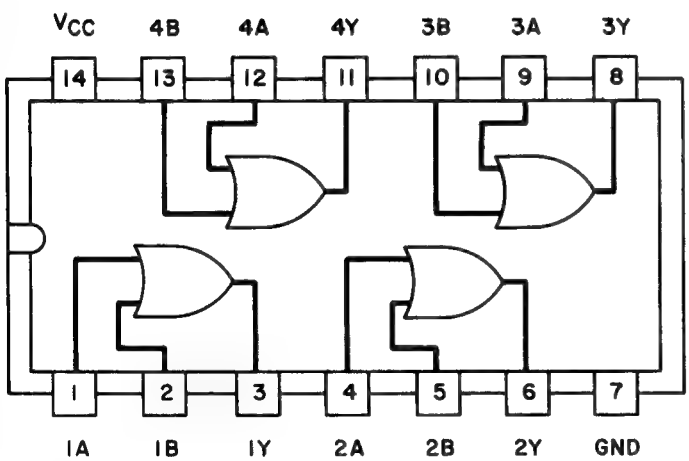
Figure 32. Quad 2-Input NOR Gate (581R500J37, M38510/00401BCB)



NOTE:

POSITIVE LOGIC, EACH GATE: $Y = A + B$

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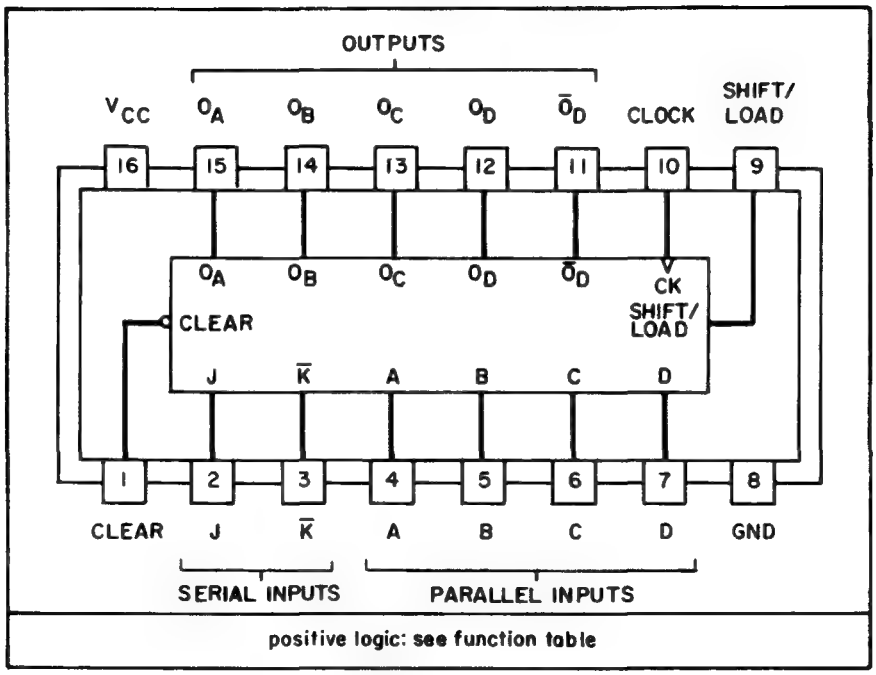
Figure 33. Quad 2-Input Positive OR Gate (581R610H01)

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



FUNCTION TABLE

INPUTS										OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL					Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D						
L	X	X	X	X	X	X	X	X		L	L	L	L	H
H	L	↑	X	X	a	b	c	d		a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X		Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}	$\overline{Q}_{DO}$
H	H	↑	L	H	X	X	X	X		Q_{AO}	Q_{AO}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X		L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X		H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X		$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at A, B, C, or D, respectively

Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C respectively, before the most-recent transition of the clock

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Figure 34. 4-Bit Shift Register (582R723H02) (Sheet 1 of 2)

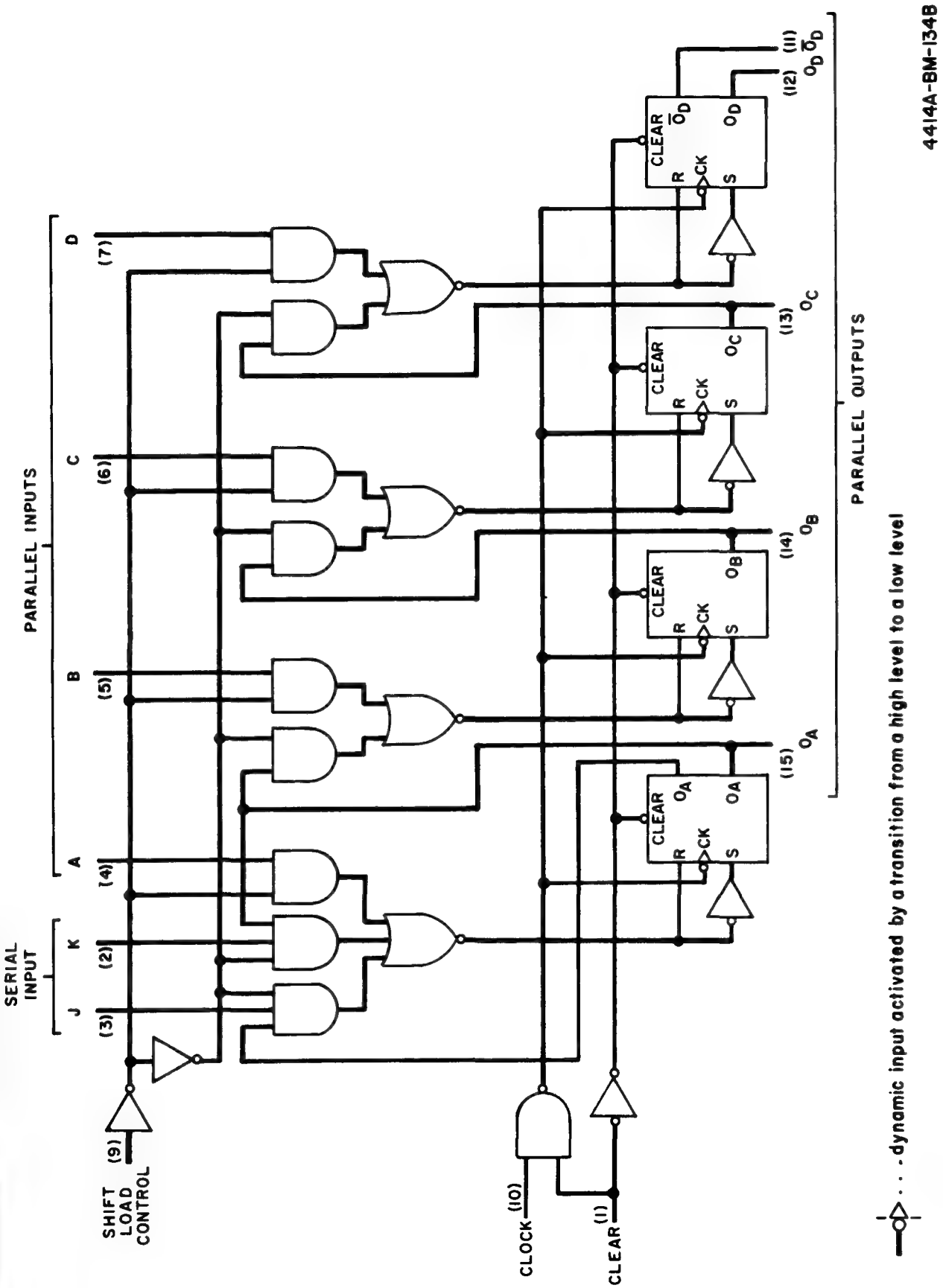


Figure 34. 4-Bit Shift Register (582R723H02) (Sheet 2 of 2)

RESISTOR	RESISTANCE OHMS	MAXIMUM CONTINUOUS WORKING VOLTAGE (SINGLE RESISTOR)
R1	220	5.74
R2	330	7.04

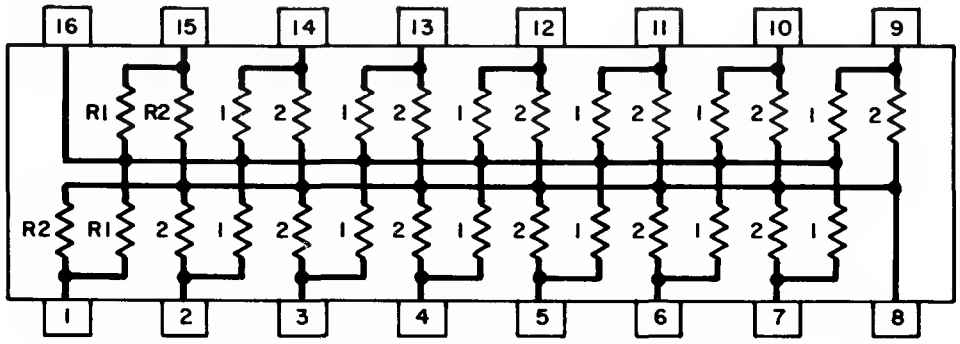
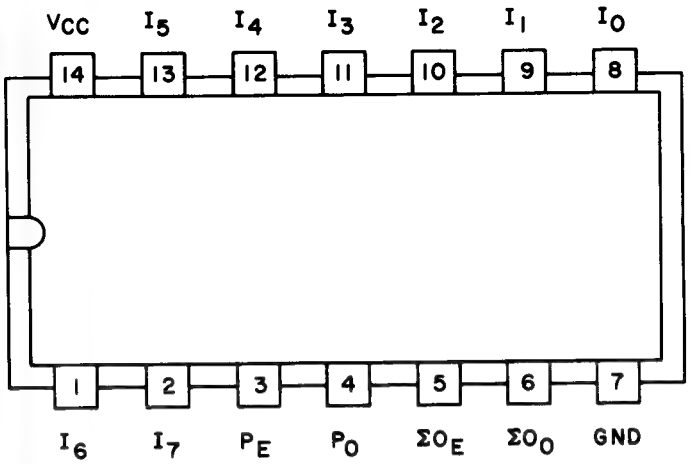


Figure 35. Resistor Network 581R871H41



TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

X = irrelevant

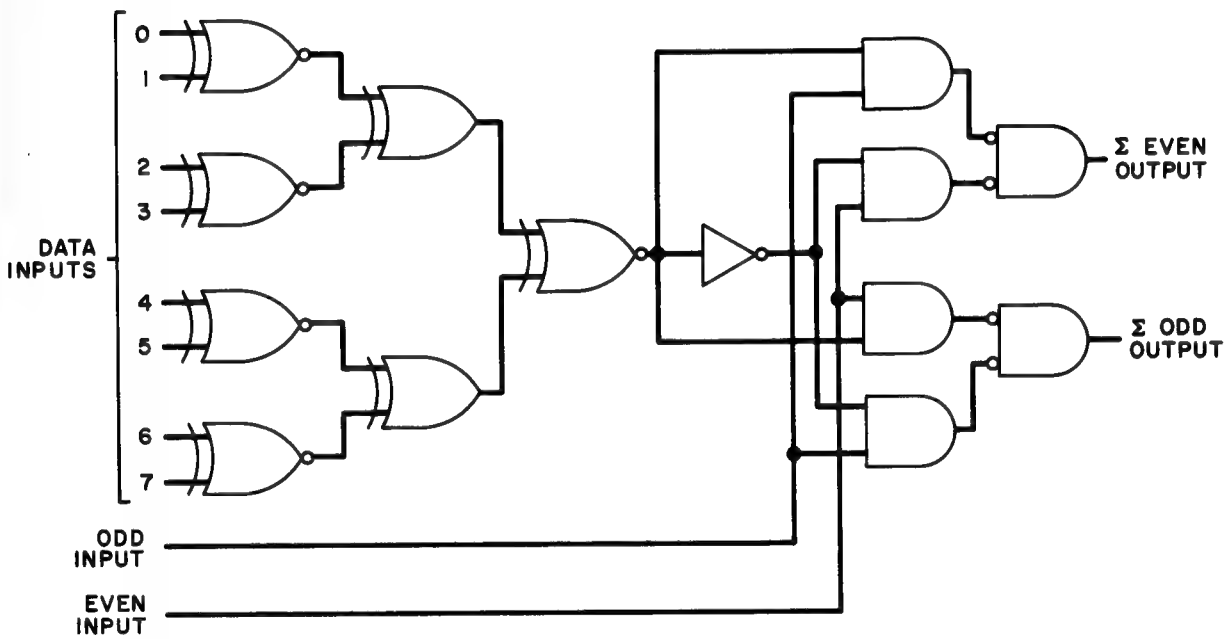


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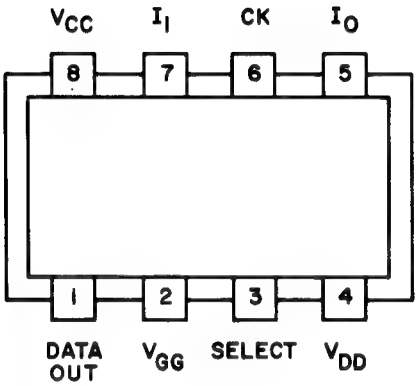
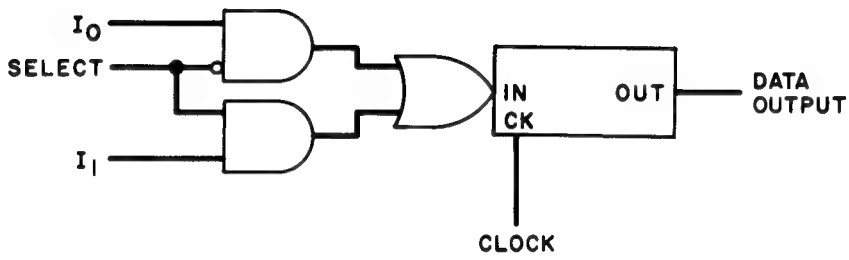
Figure 36. 8-Bit Odd/Even Parity Generator/Checker (581R825H01) (Sheet 1 of 2)

The monolithic 8-bit parity genrator/checker has control inputs and even/odd outputs to enhance operation in either odd or even parity. Cascading these circuits allows unlimited word length expansion. It is used to generate and check parity on data being transmitted from one register to another.

Figure 36. 8-Bit Odd/Even Parity Generator/Checker (581R825H01) (Sheet 2 of 2)





FUNCTION TABLE

SELECT	I_o	I_1	DATA ENTERED
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

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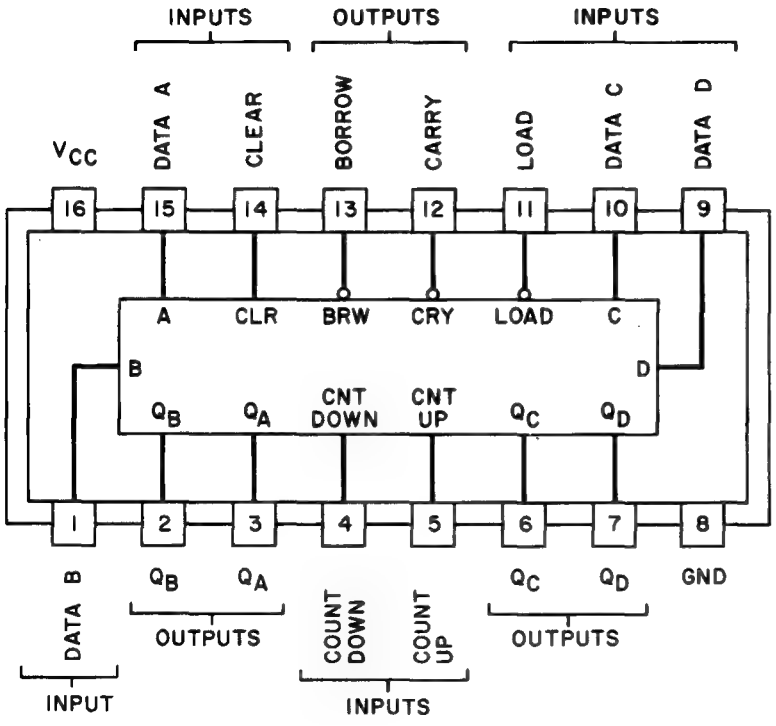
Figure 37. 1024-Bit Static Shift Register (649A888H01) (Sheet 1 of 2)

The 649A888H01 is a quasi-static 1024-bit MOS shift register using low-threshold P-channel silicon gate technology. A static shift register is capable of maintaining stored data without being continuously clocked. The static shift register is constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The device has a single TTL/DTL compatible clock input (pin 6). Data in the register is stored in static, cross-coupled latches while the clock is LOW, so that the clock may be stopped indefinitely in the LOW state. There are limitations on the time it may reside in the HIGH state. When the clock shifts from LOW to HIGH to LOW, a dynamic transfer of data occurs from one static latch to the next. The input of the register is a two-input multiplexer with both data inputs available. A select line (S) determines whether data will be accepted from the I input (Select=LOW) or the I input (Select=HIGH). The register can be placed in the recirculate mode by tying the output (pin 1) to one of the data inputs, and using the select line as a write/recirculate control.

Figure 37. 1024-Bit Static Shift Register (649A888H01) (Sheet 2 of 2)



NOTE:
"See description on next page."

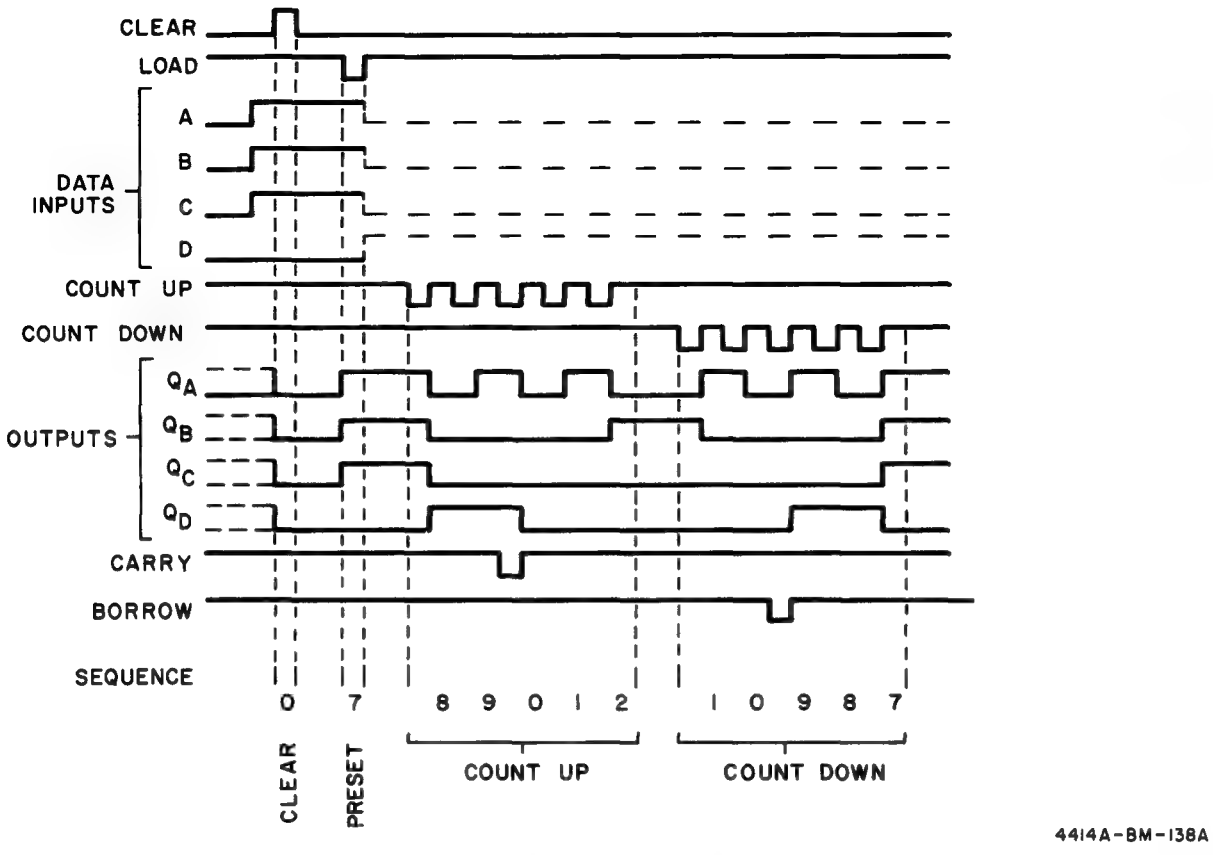


Figure 38. Synchronous 4-Bit Up/Down BCD Decade Counter (581R500J53, 128C830H13) (Sheet 1 of 3)

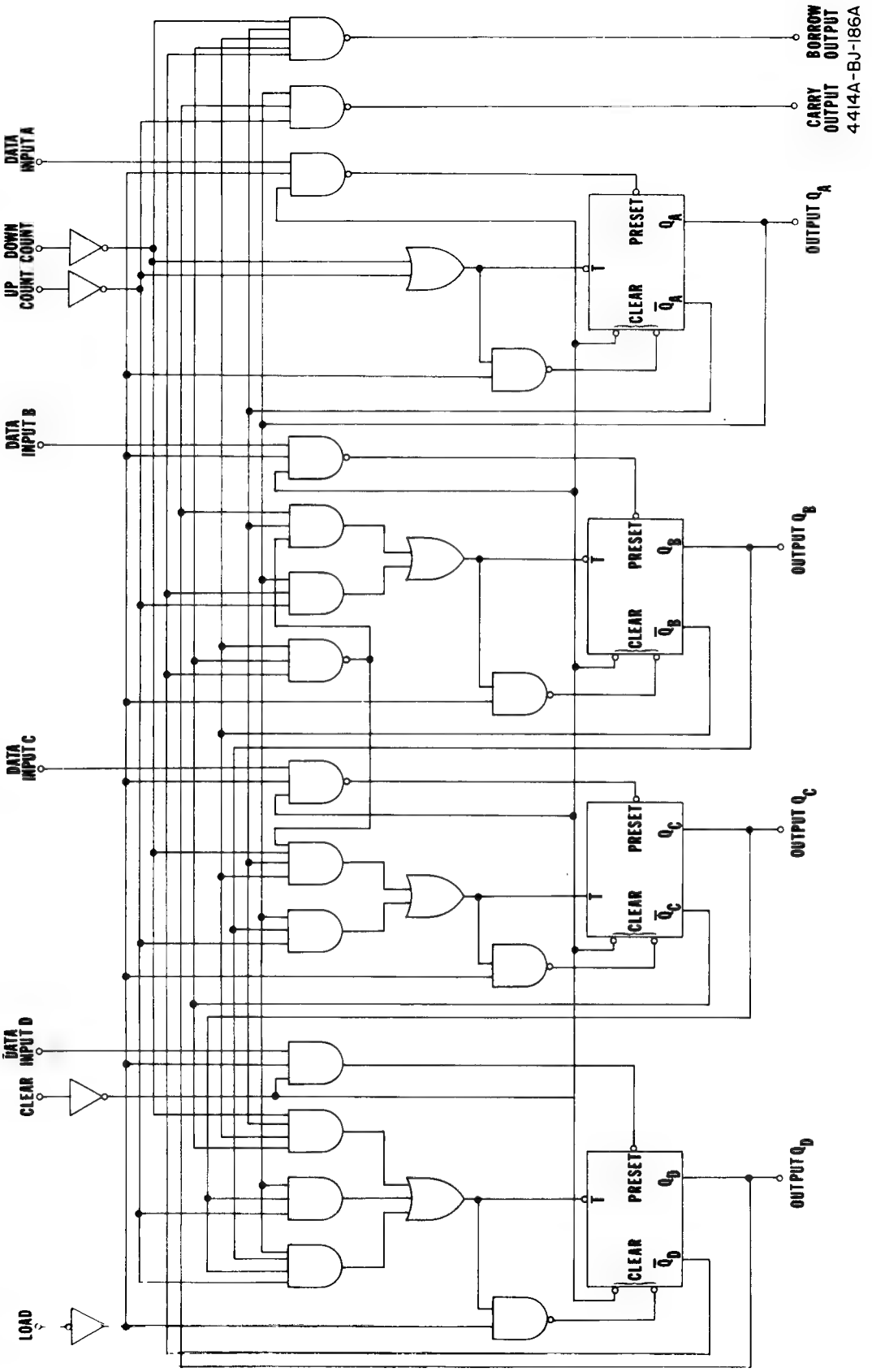
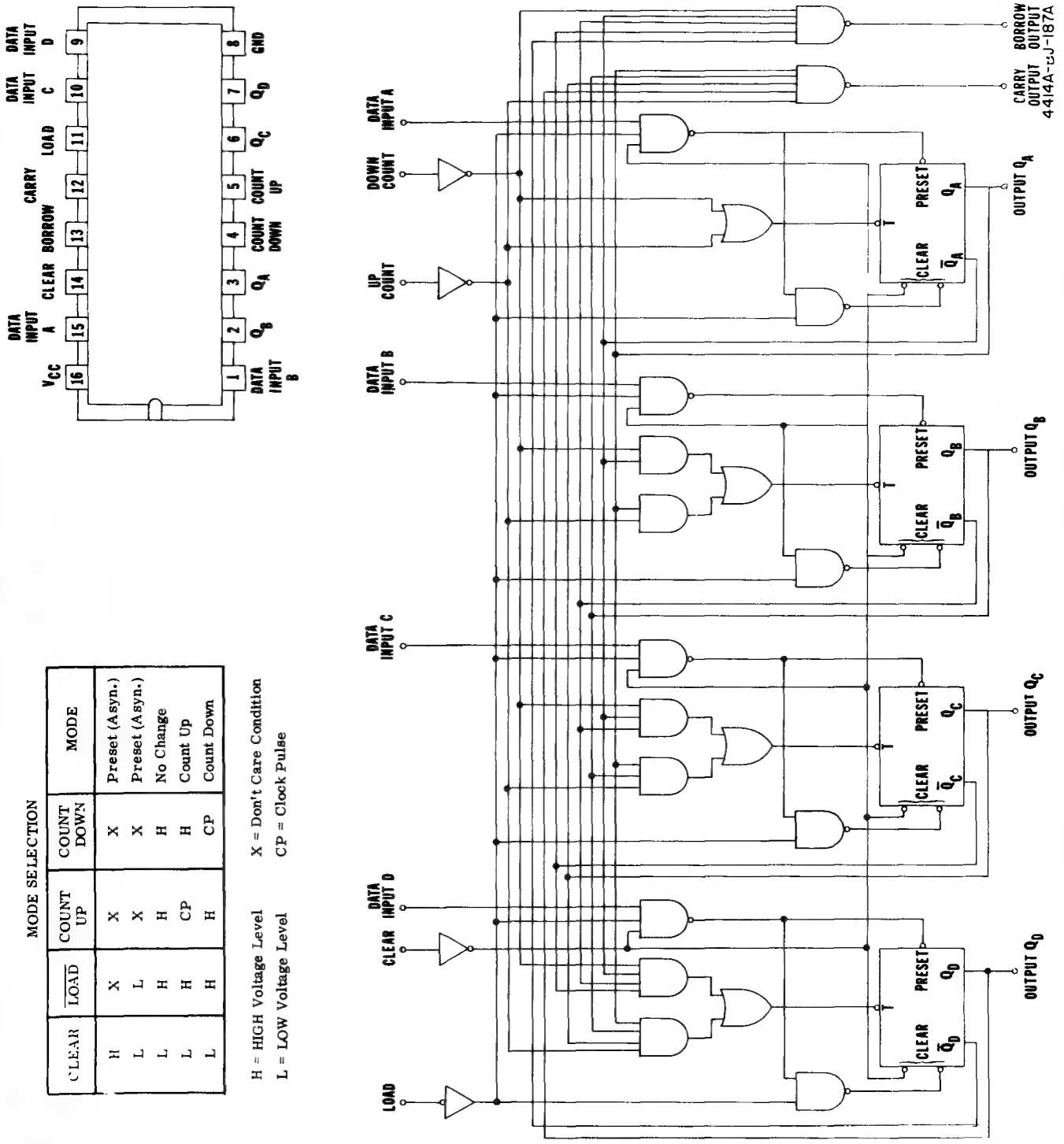


Figure 38. Synchronous 4-Bit Up/Down BCD Decade Counter (581R500J53, 128C830H13) (Sheet 2 of 3)

The preceding counter timing chart follows this sequence: clear all outputs to zero; preset the counter (load program) to BCD seven; count up to 8, 9, carry, 0, 1, 2; change command clock and count down from 2 to 1, 0, borrow, 9, 8, 7. Each of the 4 F-F's are independently presettable. A low on pin 11 (load) will set Q_A to A, Q_B = B, Q_C = C, and Q_D will follow input D. Synchronous counting occurs on a low-to-high clock transition. The clock input (pin 4 or pin 5) also determines an up or down BCD count. The unused clock input must remain high. A clear command (high to pin 14) is nonsynchronous and overrides all other action.

Figure 38. Synchronous 4-Bit Up/Down BCD Decade Counter (581R500J53, 128C830H13) (Sheet 3 of 3)

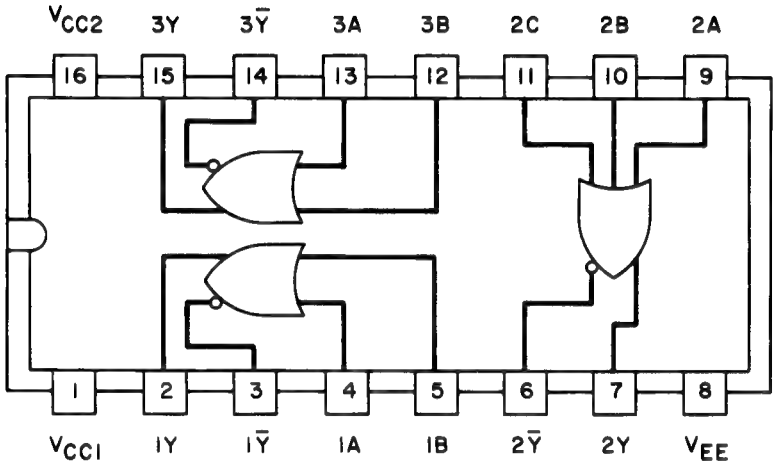


MODE SELECTION

CLEAR	$\overline{\text{LOAD}}$	COUNT UP	COUNT DOWN	MODE
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

H = HIGH Voltage Level X = Don't Care Condition
L = LOW Voltage Level CP = Clock Pulse

Figure 39. Synchronous 4-Bit Up/Down Binary Counter with Preset Inputs (581R500J12, 128C830H14)



NOTE:
POSITIVE LOGIC
$Y = A + B + C$
$\overline{Y} = \overline{A + B + C}$
NEGATIVE LOGIC
$Y = ABC$
$\overline{Y} = \overline{ABC}$

INPUTS			OUTPUTS	
A	B	C	Y	$\overline{Y}$
L	L	L	L	H
X	X	H	H	L
X	H	X	H	L
H	X	X	H	L

The device illustrated is a positive logic OR/NOR triple gate. It can also be used as a negative logic AND/NAND gate. Each ECL gate has both OR and NOR emitter-follower outputs. The OR function can be expanded (the number of inputs increased) by wiring the emitter-follower outputs of individual gates together.

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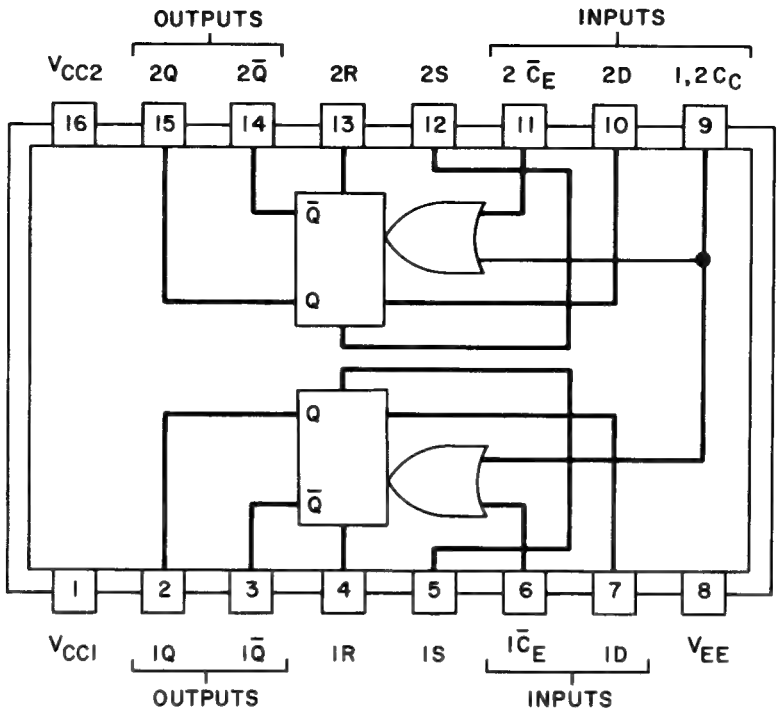
Figure 40. Triple 2-3-2-Input OR/NOR Gate (581R688H07)



CLOCKED TRUTH TABLE

D	C_C	$\overline{C}_E$	Q_{N+1}	$\overline{Q}_{N+1}$
L	L	L	Q_N	$\overline{Q}_N$
L	L	H	Q_N	$\overline{Q}_N$
L	H	L	L	H
L	H	H	Q_N	$\overline{Q}_N$
H	L	L	Q_N	$\overline{Q}_N$
H	L	H	Q_N	$\overline{Q}_N$
H	H	L	H	L
H	H	H	Q_N	$\overline{Q}_N$

R-S TRUTH TABLE

R	S	Q^{N+1}	$\overline{Q}^{N+1}$
L	L	Q^N	$\overline{Q}^N$
L	H	H	L
H	L	L	H
H	H	N.D.	N.D.

NOTES:
1. Positive logic: H = high voltage level L = low voltage level
2. An H on clock terminal C_C represents a transition from low to high state between T_N and T_{N+1} while terminal $\overline{C}_E$ is static.
3. N. D. = not defined
4. Q^N = status of "Q" output prior to application of R-S inputs specified.
5. Q^{N+1} = status of "Q" output after application of R-S inputs specified.
6. Q_N = status of "Q" output prior to application of leading edge of positive going clock pulse.
7. Q_{N+1} = status of "Q" output after application leading edge of positive going clock pulse.
8. Truth tables apply to each flip-flop.
9. Asynchronous set (S) and reset (R) inputs override each clock input.

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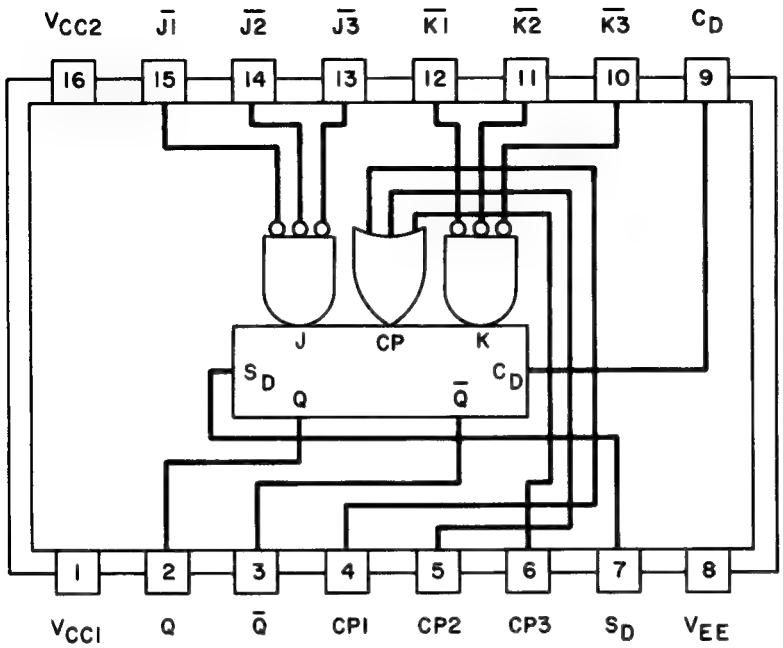
Figure 41. Dual D-type Master-Slave Flip-Flop (138C439H01)



TRUTH/FUNCTION TABLE

SYNCHRONOUS TRUTH TABLE

$\overline{J}$ 2/	$\overline{K}$ 2/	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	$\overline{Q}_n$	Q_n
L	H	H	L
H	L	L	H
H	H	Q_n	Q_n

ASYNCHRONOUS TRUTH TABLE

C_D	S_D	Q	$\overline{Q}$
L	L	SYNCHRONOUS	
L	H	H	L
H	L	L	H
H	H	UNDETERMINED	

NOTES: 1. POSITIVE LOGIC: H = V_{ih} FOR INPUTS, V_{oh} FOR OUTPUTS
L = V_{il} FOR INPUTS, V_{ol} FOR OUTPUTS

2. $\overline{J} = \overline{J_1} + \overline{J_2} + \overline{J_3}$
$\overline{K} = \overline{K_1} + \overline{K_2} + \overline{K_3}$

3. Q OR $\overline{Q}$ IS THE LEVEL OF THE Q OR $\overline{Q}$ OUTPUT PRIOR TO A LOW TO HIGH TRANSITION OF THE CLOCK INPUT (CP_1 OR CP_2 OR CP_3).

4. Q_{n+1} OR $\overline{Q}_{n+1}$ IS THE LEVEL OF THE Q OR $\overline{Q}$ OUTPUT AFTER ONE LOW TO HIGH TRANSITION OF THE CLOCK INPUT (CP_1 OR CP_2 OR CP_3).

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Figure 42. J-K Edge-Triggered Flip-Flop 138C566H01

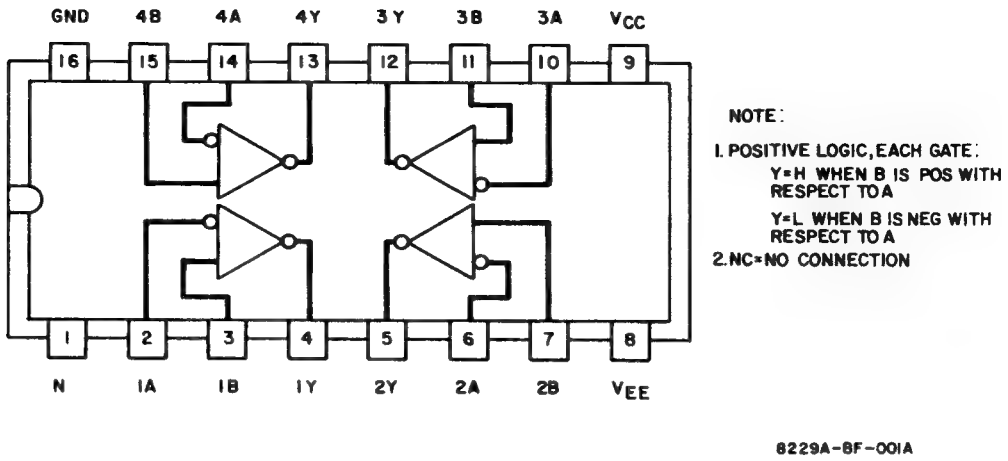


Figure 43. ECL to TTL Level Translator (583R357H02)

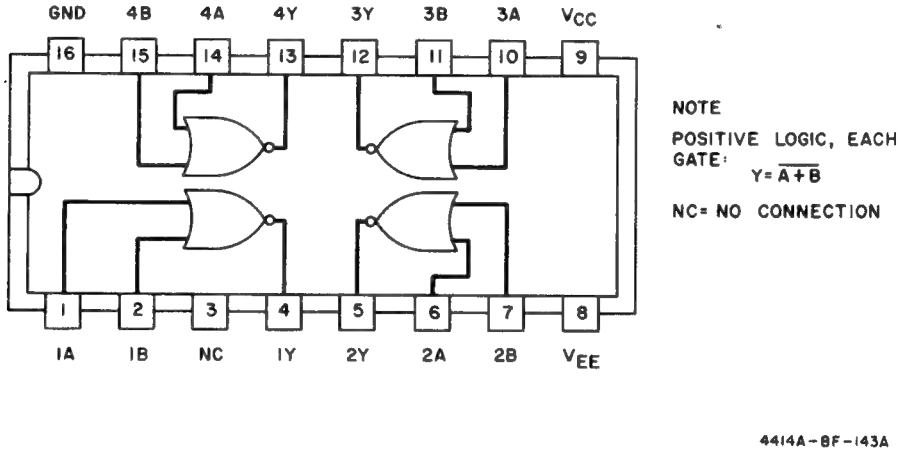


Figure 43.1. ECL to TTL Level Translator (138C461H01)

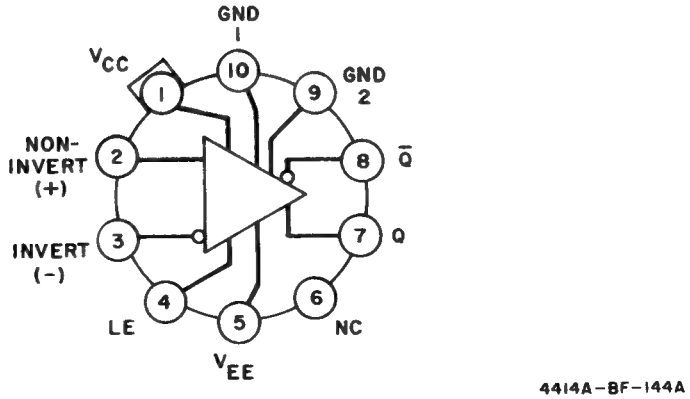


Figure 44. High-Speed Comparator with ECL Outputs (581R709H02)

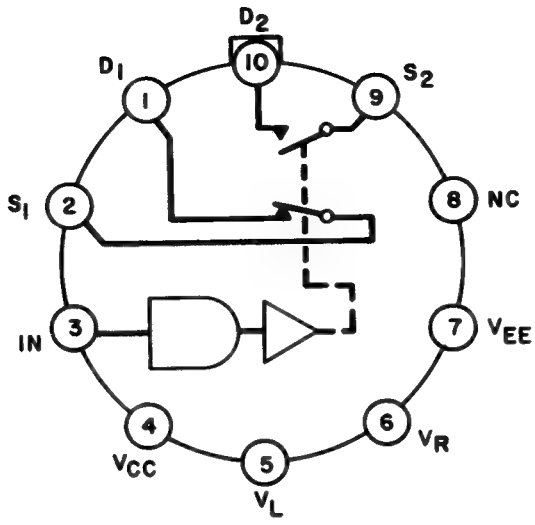


Figure 45. High-Speed Analog Gate (578R823H03)

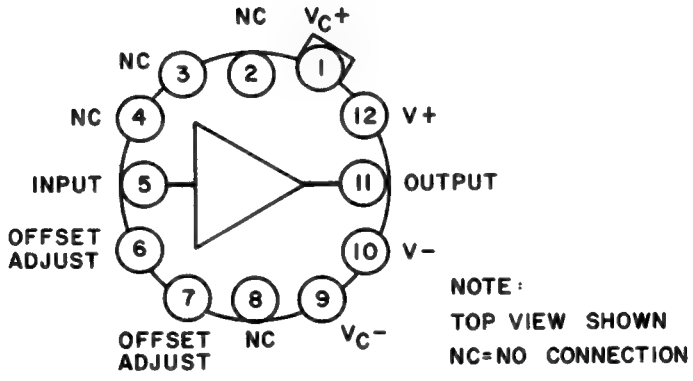
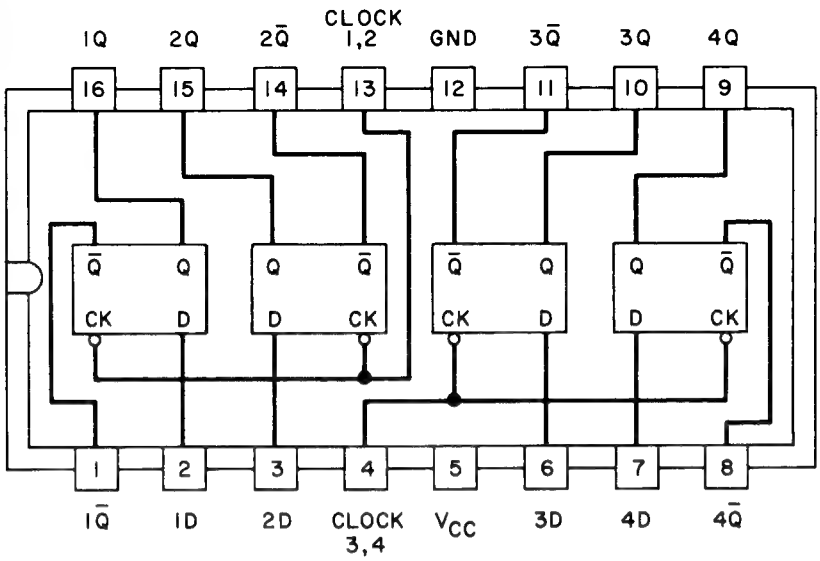


Figure 46. Analog Amplifier (581R684H01)



TRUTH TABLE (EACH LATCH)	
t_n	t_n+1
D	Q
1	1
0	0

NOTES:
1. T_n=BIT before clock pulse transition.
2. T_{n+1}=BIT after clock pulse transition.
3. D input is activated only when clock input is in "1" state.
4. Logic level definitions
   "1"=2.0Vdc(min.) } Input
   "0"=0.8Vdc(max.) }
   "1"=2.4Vdc(min.) } Output
   "0"=0.4Vdc(max.) }

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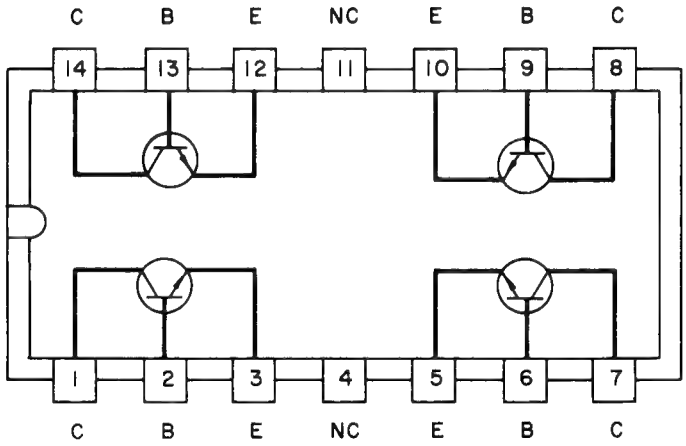
Figure 47. Quad Bistable Latch (578R644H02)



NOTE:
NC = NO CONNECTION

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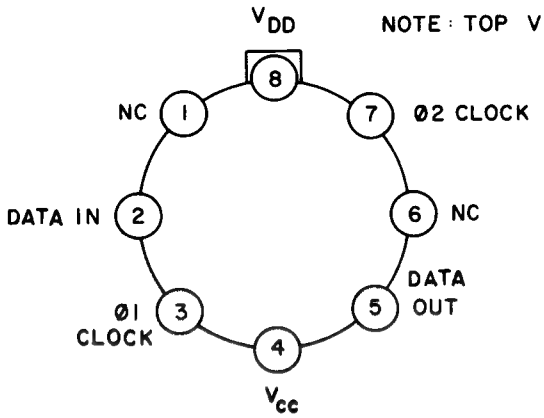
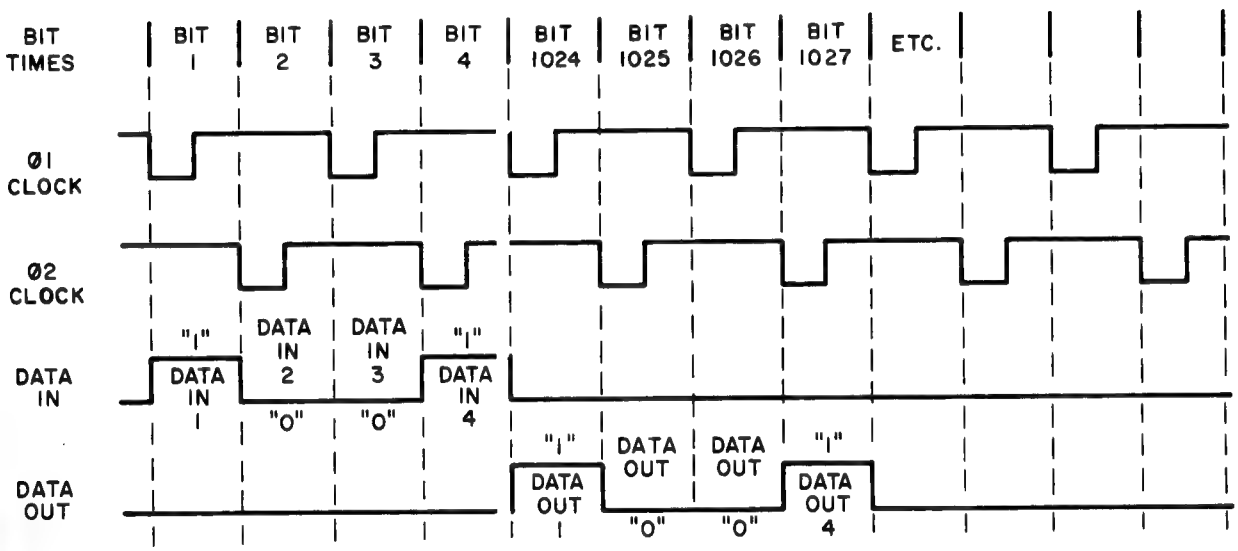
Figure 48. Quad Driver (649A808H01)



This device requires two-phase non-overlapping clocks, and provides a one-bit shift on each clock pulse.



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at $\emptyset_1$ time, it exists at $\emptyset_1$ time. (Beginning on $\emptyset_{1's}$ negative going edge and ending on the succeeding $\emptyset_{2's}$ negative going edge.)

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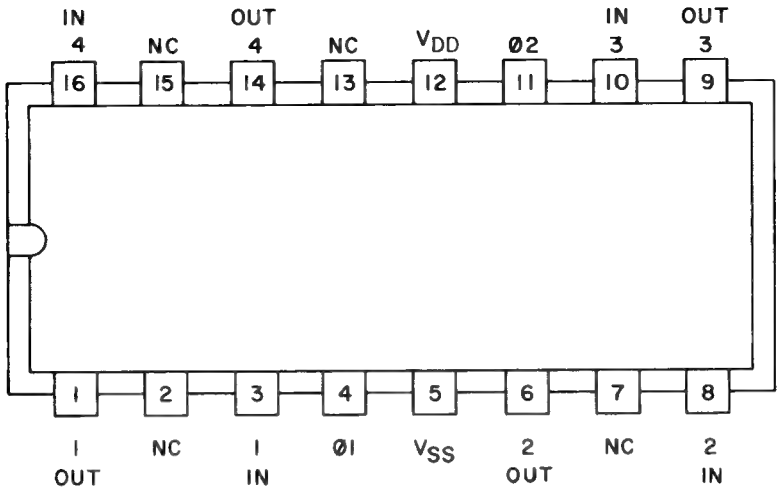
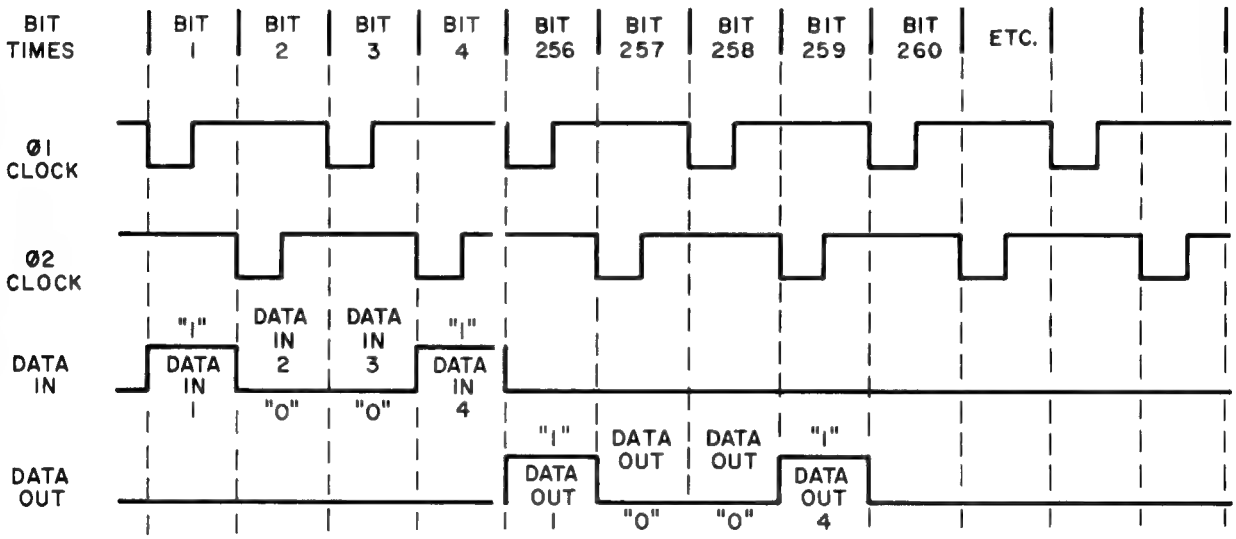
Figure 49. 1024-Bit Dynamic Shift Register (138C177H01)



NOTE:
NC = NO CONNECTION

This device requires two-phase non-overlapping clocks, and provides a one-bit shift on each clock pulse.



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exists at ϕ_1 time. (Beginning on $\phi_{1's}$ negative going edge and ending on the succeeding $\phi_{2's}$ negative going edge.)

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Figure 50. Quad 256-Bit Dynamic Shift Register (581R288H01)

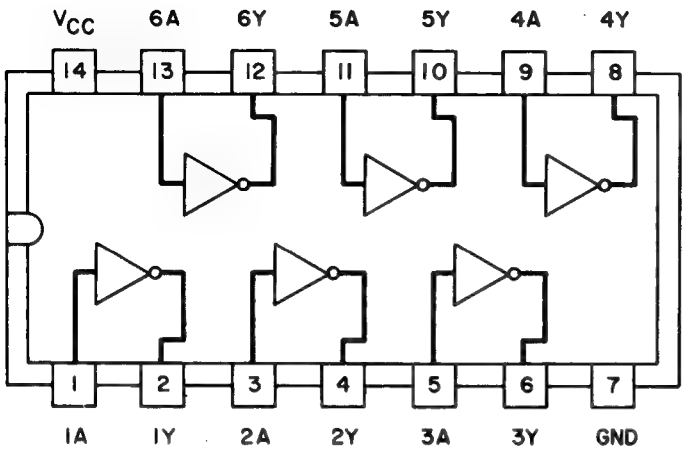

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Figure 51. Hex Inverter Buffer/Driver with Open Collector High Voltage Outputs (581R500H71, 128C829H01)

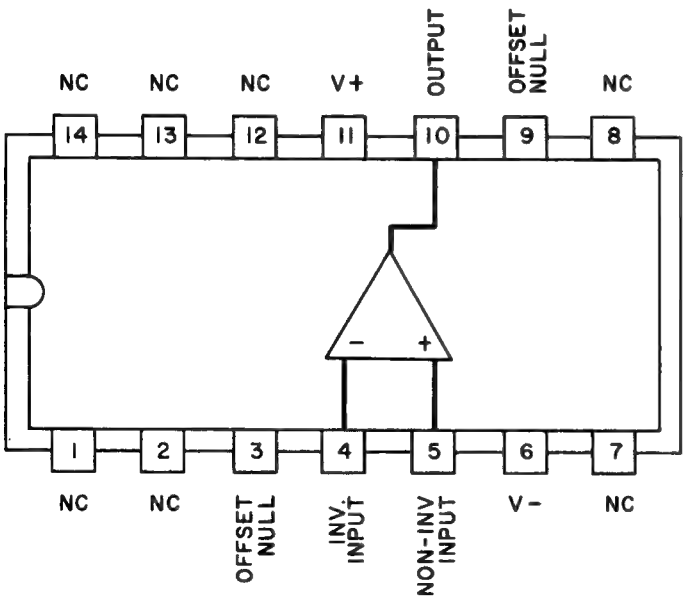

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Figure 52. Linear Operational Amplifier (M38510/10101BCB)

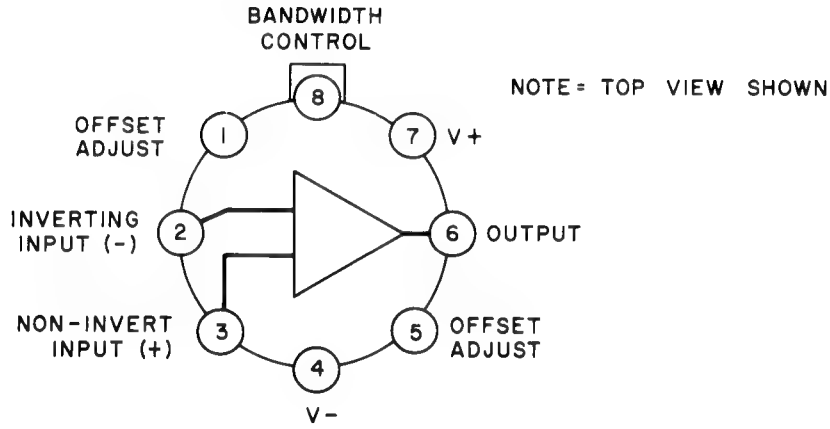

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Figure 53. Analog Operational Amplifier (142C675H01)

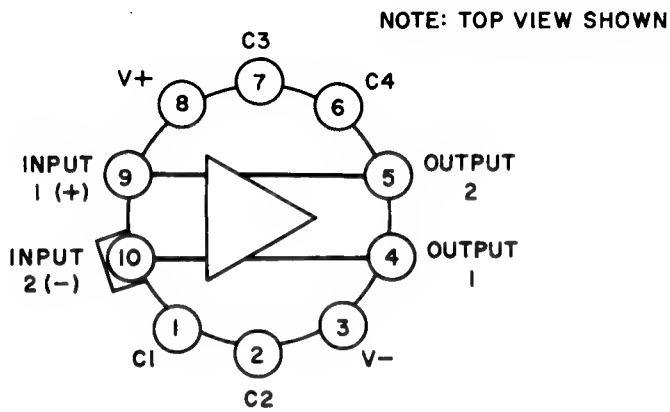

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Figure 54. Differential Video Amplifier (649A821H01)

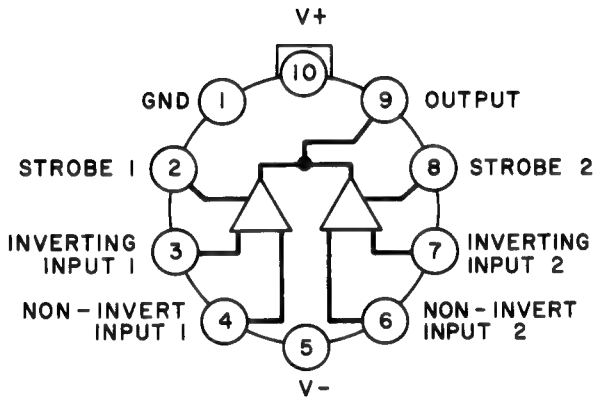

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Figure 55. Dual Linear Comparator (578R642H01)

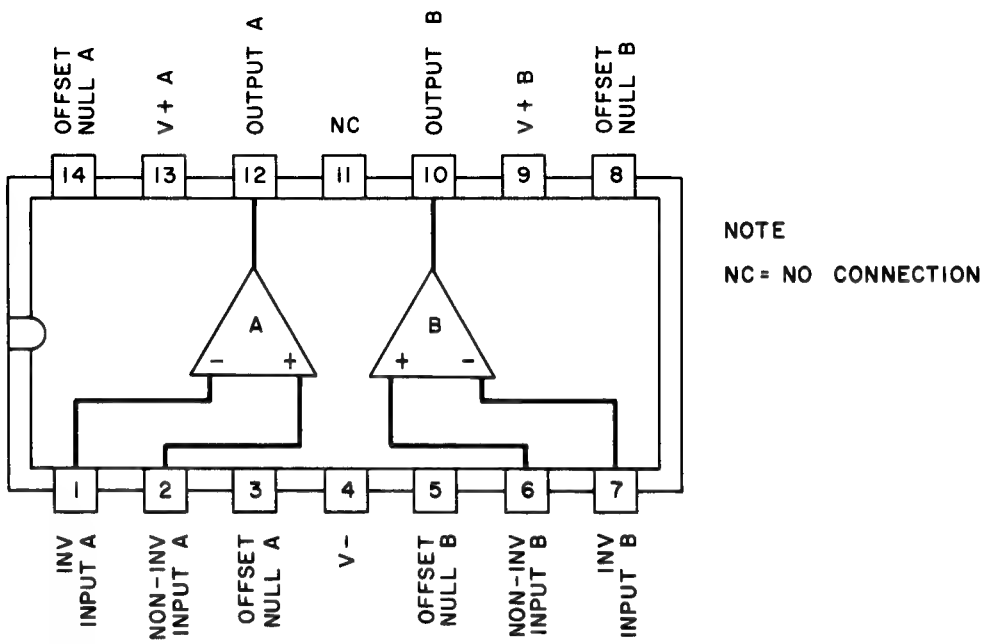

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Figure 56. Dual Linear Operational Amplifier (582R728H02)

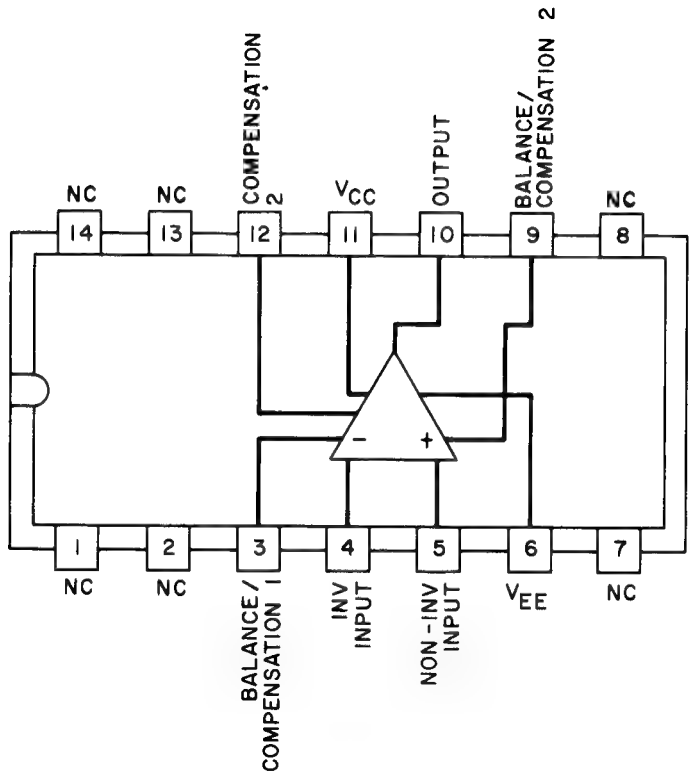
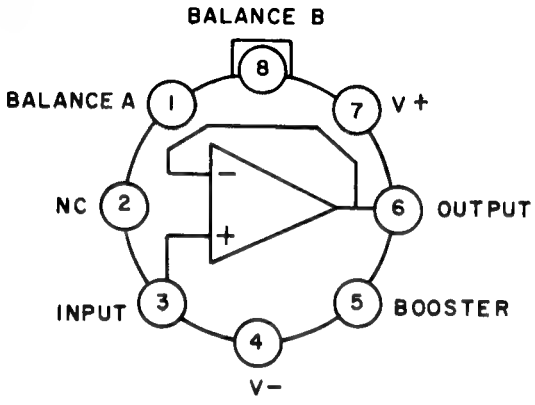


Figure 57. Analog Operational Amplifier (581R923H02)



The 581R710H02 is an operational amplifier connected internally as a unity gain non-inverting voltage follower This type of device has the advantages of low input current and high speed slew rate (rapid following of input changes). The 581R710H02 supersedes (and is interchangable with) Westinghouse PN 581R500J11.

Figure 58. Operational Amplifier (581R710H02)

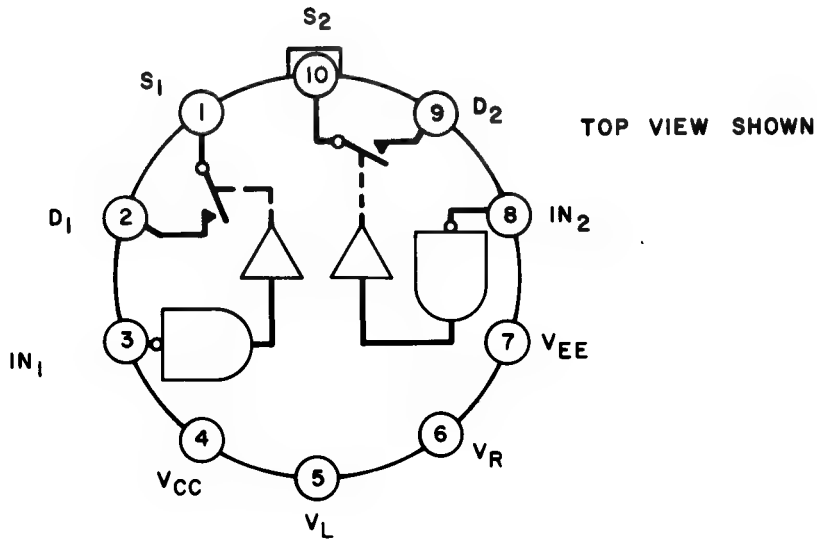
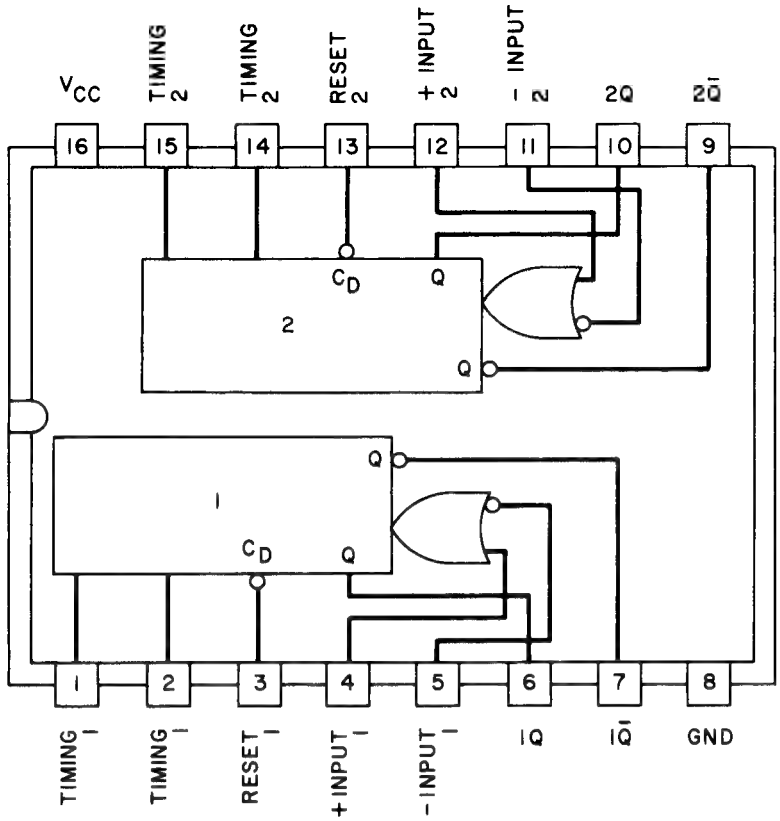


Figure 59. Dual SPST Analog Gate (578R823H05)



TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	Operation
H L	L	H	Trigger
H	L H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level $\geq V_{1H}$
L = LOW Voltage Level $\leq V_{1L}$
X = Don't Care
H L = HIGH to LOW Voltage Level transition
L H = LOW to HIGH Voltage Level transition

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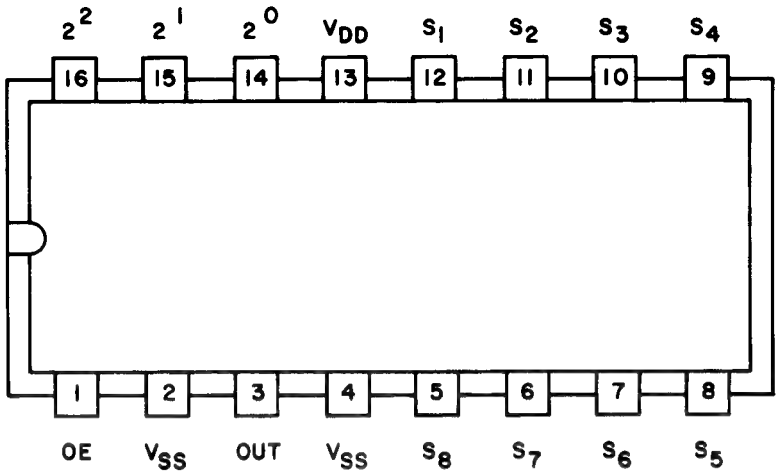
Figure 60. Dual Digital-to-TTL Monostable Multivibrator (578R601H01)



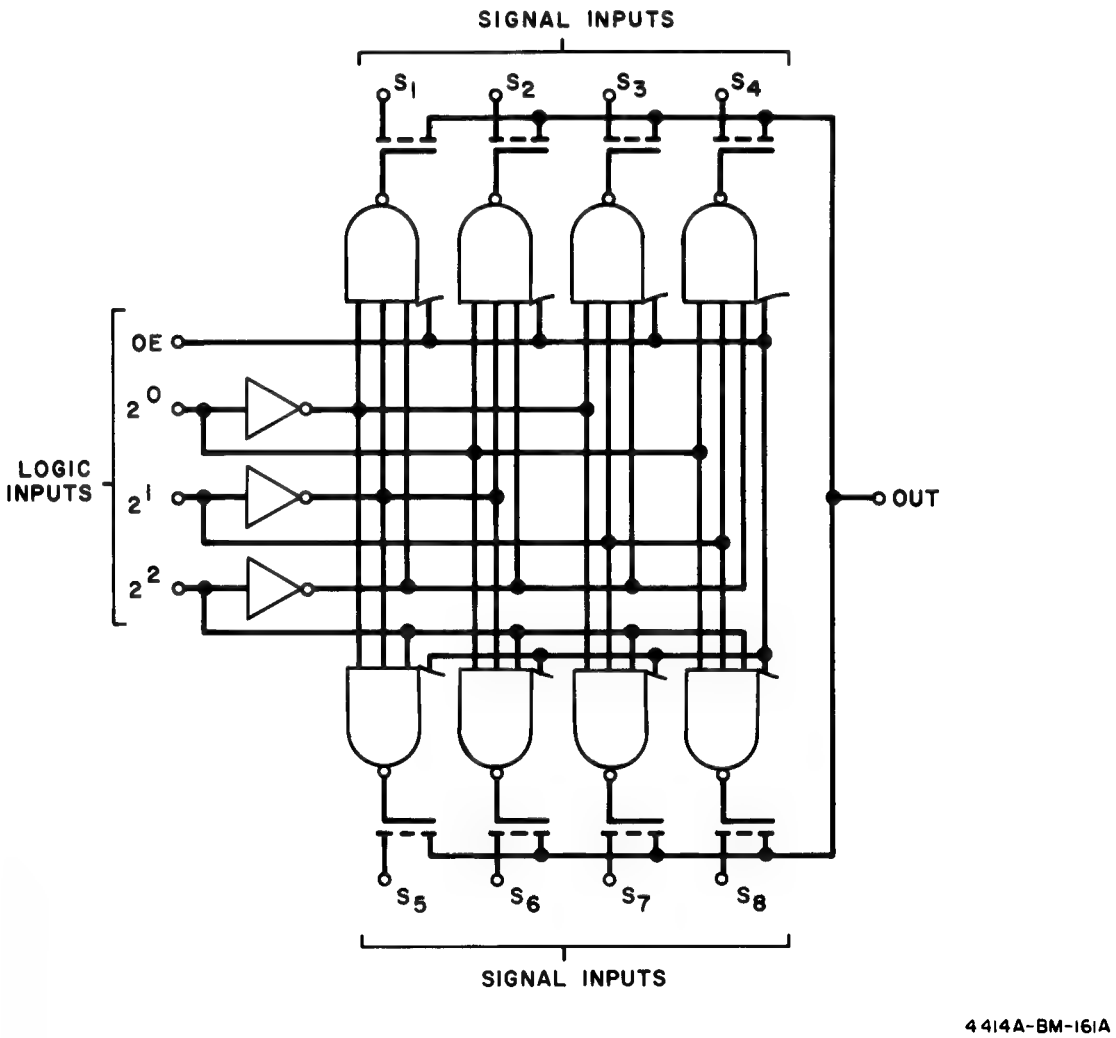


Figure 61. Analog Multiplex Switch, 8-Channel MOS (581R803H01) (Sheet 1 of 2)

TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

NOTES: 1. Logic inputs; the logic levels shall be: $L \leq V_{SS}$-4.0Vdc, $H \geq V_{SS}$-1.5Vdc.

2. S_N "ON"; In each case, the inter terminal resistance shall be $\leq$ 400 ohms at any voltage between -5.0 Vdc and 5.0 Vdc.

3. S_N "OFF"; In each case the inter terminal resistance shall be $\geq 1.5 \times 10^9$ ohms at any voltage between -5.0 Vdc and 5.0 Vdc.

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Figure 61. Analog Multiplex Switch, 8-Channel MOS (581R803H01) (Sheet 2 of 2)

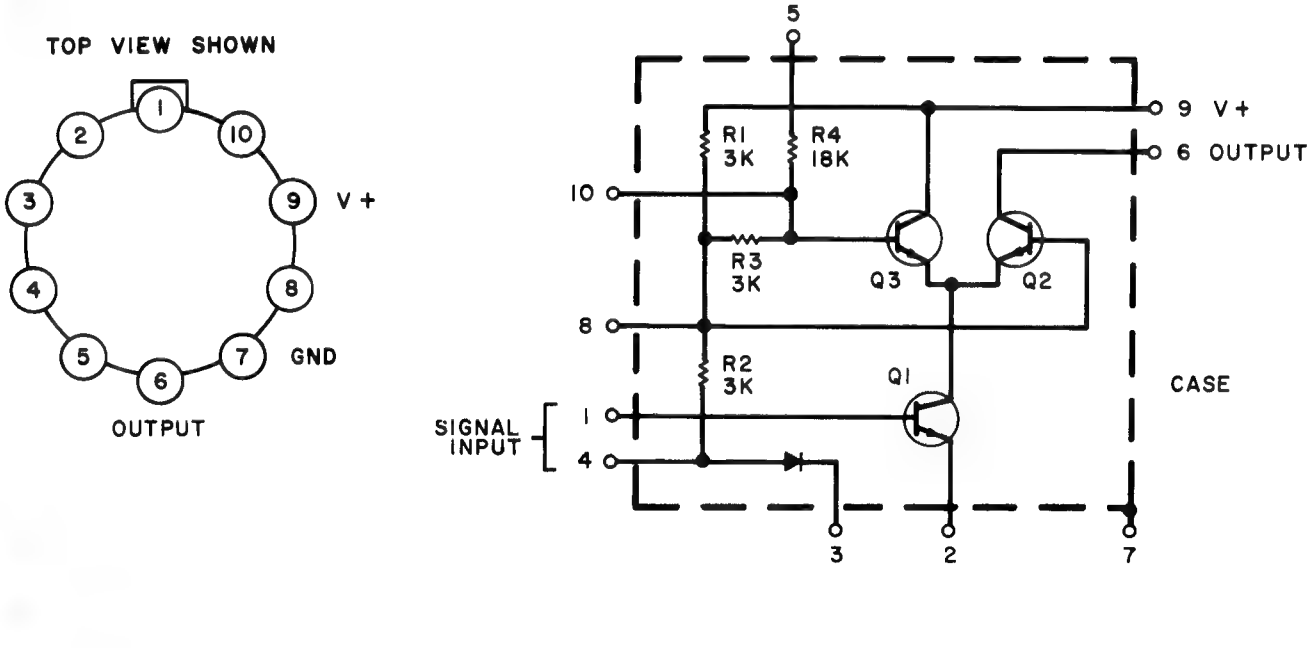

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Figure 62. Analog RF-IF Amplifier (578R765H02)

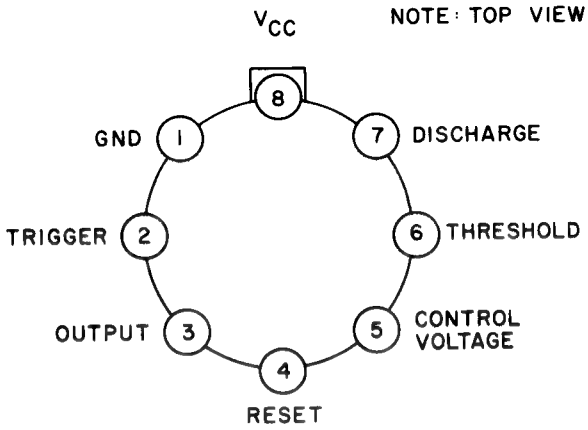

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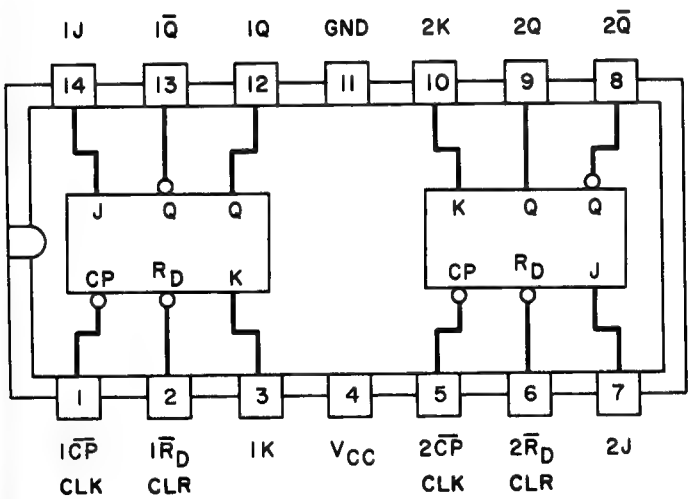
Figure 63. Analog Timer (142C516H01)



TRUTH TABLE

INPUTS (t_n)				OUT (t_n+1)		
CLEAR	CLOCK	J	K	Q	$\overline{Q}$	
LOW	X	X	X	L	H	
H	↓	L	L	Q_n	$\overline{Q_n}$	①
H	↓	L	H	L	H	
H	↓	H	L	H	L	
H	↓	H	H	$\overline{Q_n}$	Q_n	②

① Remains unchanged
② Toggles

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
↓ = falling edge of clock pulse

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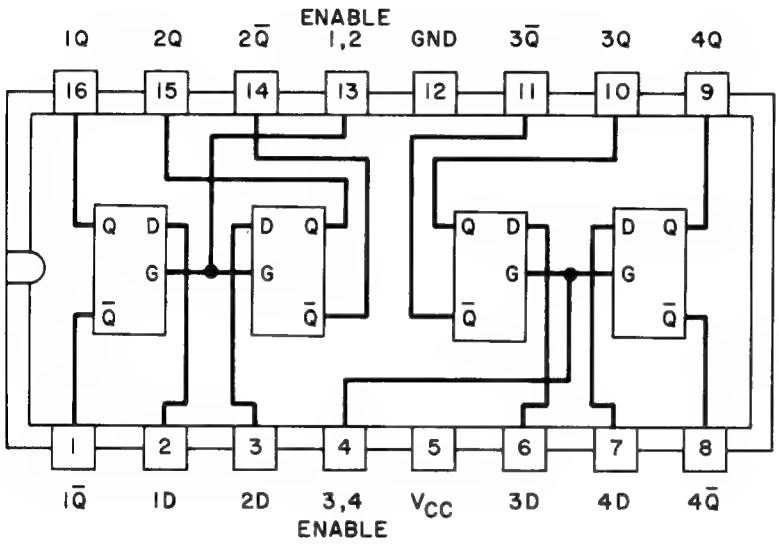
Figure 64. Dual J-K Master-Slave Flip-Flop (128C823H02)



FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = high level, L =low level, X =irrelevant
Q_0 = the level of Q before the high-to-low transition of G

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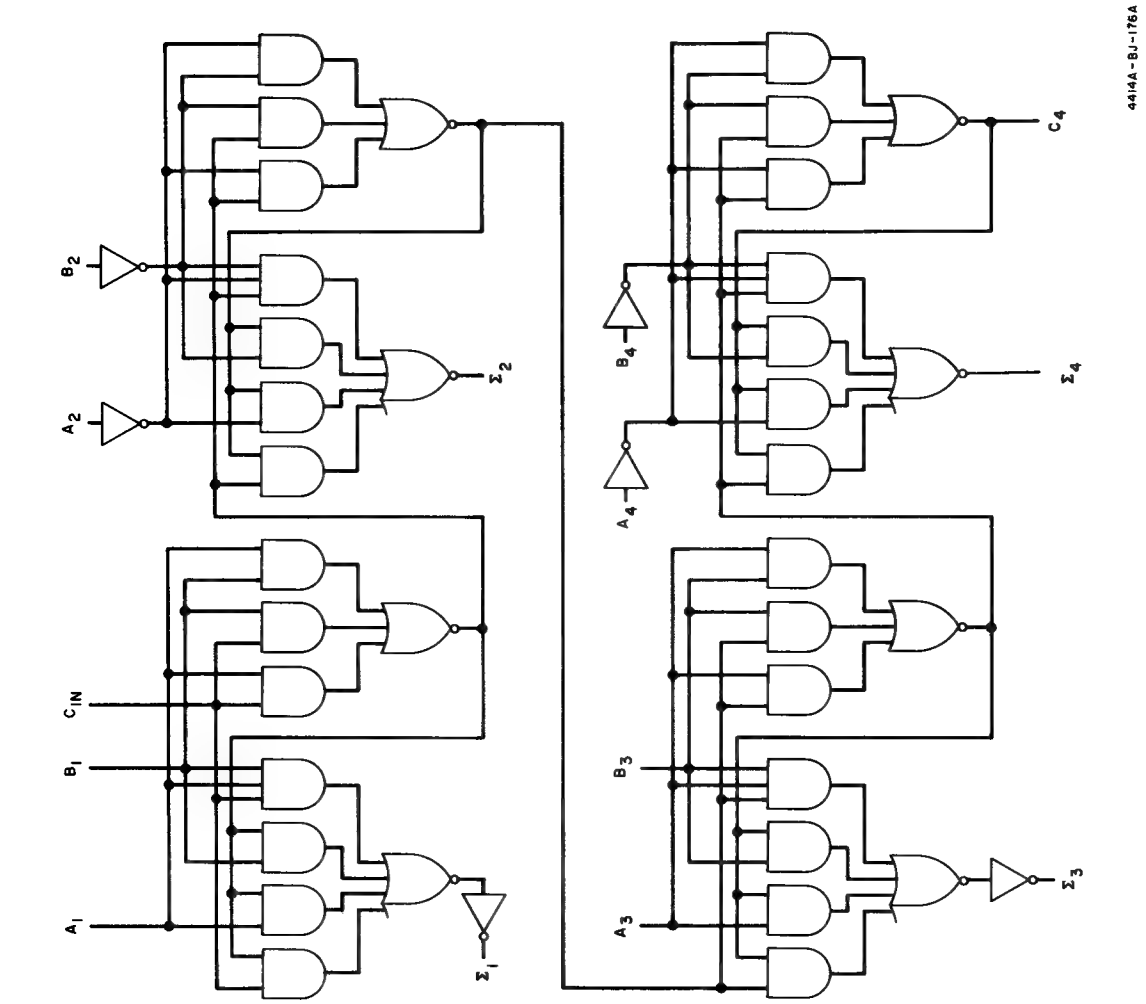
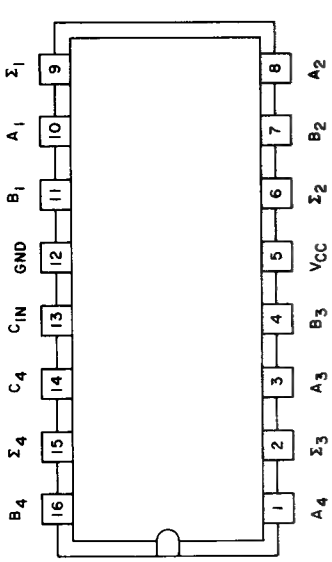
Figure 65. 4-Bit Bistable Latch (128C830H02)

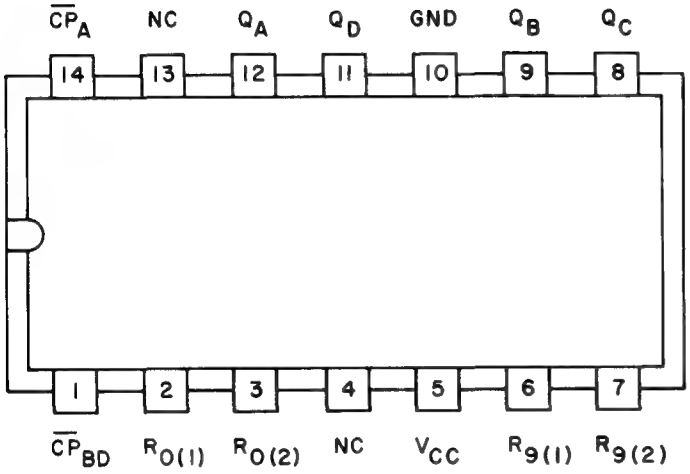




INPUT					OUTPUT							
					WHEN C_{IN} = 0				WHEN C_{IN} = 1			
							WHEN C_2 = 0				WHEN C_2 = 1	
A1 A3	B1 B3	A2 A4	B2 B4	C_{IN}	Σ_1	Σ_3	Σ_2	Σ_4	C2	C4	Σ_1	Σ_3	Σ_2	Σ_4	C2	C4
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	H	H	L	L	L
H	H	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L
L	L	H	L	L	L	H	H	L	L	L	H	L	H	H	L	L
H	L	H	L	L	H	H	H	L	L	L	L	H	H	H	L	L
L	H	H	L	L	H	H	L	H	L	L	L	H	L	H	H	L
H	H	H	L	L	L	L	L	H	H	L	L	H	L	H	H	L
L	L	L	H	L	L	H	L	H	L	L	H	L	L	L	L	H
H	L	L	H	L	H	H	L	H	L	L	L	H	L	L	L	H
L	H	L	H	L	H	H	H	H	L	L	L	H	L	L	L	H
H	H	L	H	L	L	L	H	H	L	H	L	H	L	L	L	H
L	L	H	H	L	L	H	H	H	L	H	L	H	L	H	H	H
H	L	H	H	L	H	H	H	H	L	H	L	H	L	H	H	H
L	H	H	H	L	H	H	L	H	H	H	L	H	L	H	H	H
H	H	H	H	L	L	L	L	H	H	H	L	H	L	H	H	H

NOTE:
1. Input conditions at A_1, A_2, B_1, B_2 and C_{IN} are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4 and C_4.

Figure 66. 4-Bit Binary Full Adder (128C830H03)



TRUTH TABLES

BCD COUNT SEQUENCE (Note 1)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

RESET/COUNT (see Note 2)

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{g(1)}$	$R_{g(2)}$	Q_D Q_C Q_B Q_A
H	H	L	X	L L L L
H	H	X	L	L L L L
X	X	H	H	H L L H
X	L	X	L	COUNT
L	X	L	X	COUNT
L	X	X	L	COUNT
X	L	L	X	COUNT

NOTES
1. Output Q_A connected to input CP_{BD} for BCD count.
2. X indicates that either a HIGH level or a LOW level may be present.

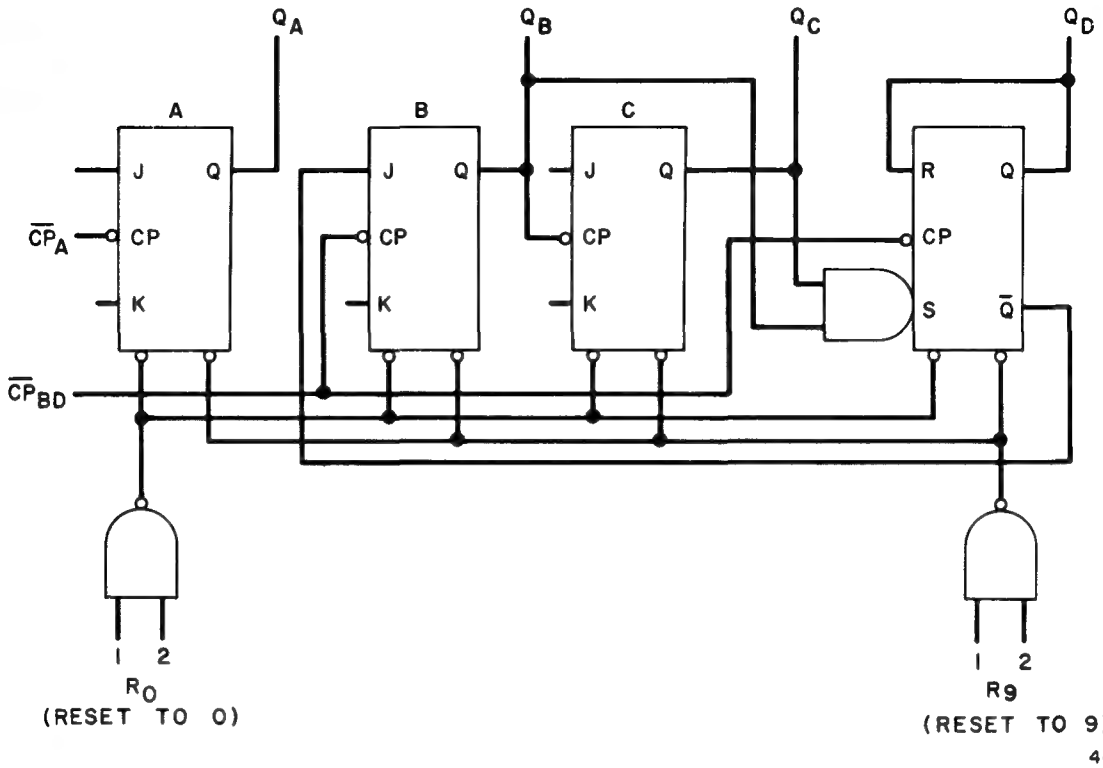
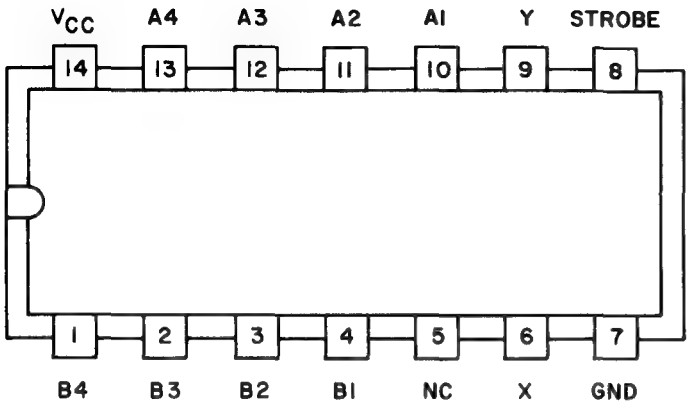


Figure 67. Decade Counter (128C955H01)



NOTE:

NC= NO CONNECTION

TRUTH TABLE

INPUT			OUTPUT	
An	Bn	STROBE	X	Y
A > B		0	1	0
A < B		0	0	1
A = B		0	1	1
A = B		1	0	0

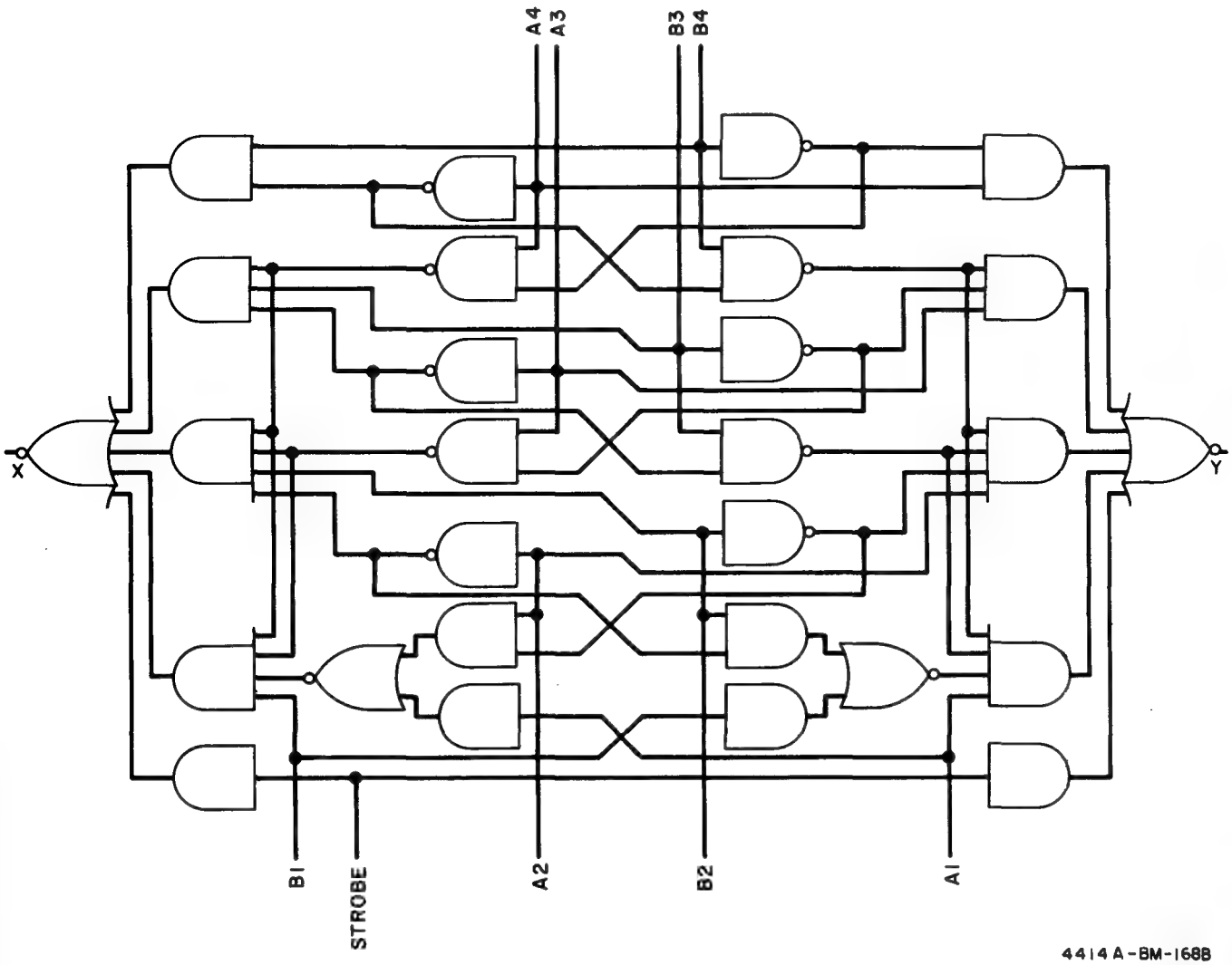
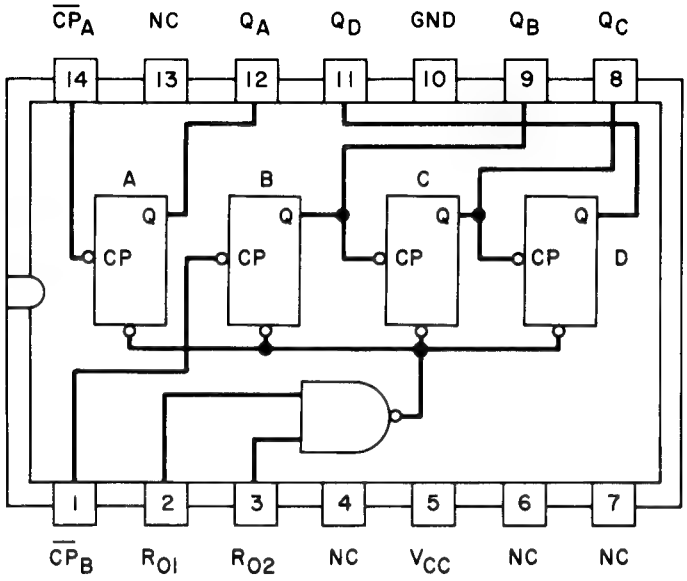


Figure 68. 4-Bit Comparator (128C921H01)



NOTE:
NC = NO CONNECTION

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

This device can be used as a divide-by-two (using flip-flop A, only), divide-by-eight (using sections B, C, and D), or as a divide-by-sixteen counter (using all 4 flip-flops). The device operates on a falling edge clock entering pin 14 (÷2 or ÷16) or pin 1 (÷8). To divide by sixteen (as shown in the truth table), output pin 12 must be connected to clock input pin 1. R_{01} or R_{02} (or both) must be low for the device to count.

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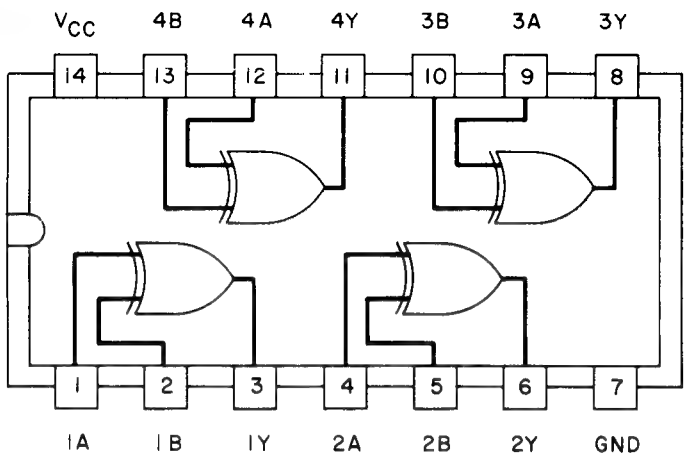
Figure 69. 4-Bit Binary Counter (128C830H05)



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

NOTE:
POSITIVE LOGIC:
$Y = A + B = \bar{A}B + A\bar{B}$

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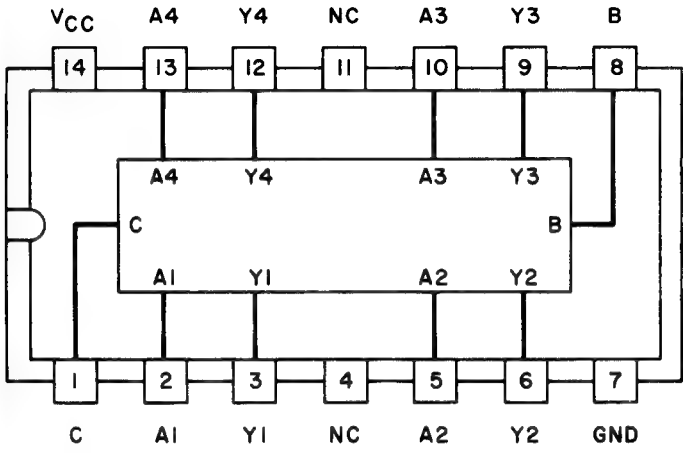
Figure 70. Quad 2-Input Exclusive OR Gate (128C821H12)



CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
0	0	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
0	1	A1	A2	A3	A4
1	0	1	1	1	1
1	1	0	0	0	0

NOTE

POSITIVE LOGIC

NC= NO CONNECTION

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Figure 71. 4-Bit True Complement with Zero/One Element (128C830H04)

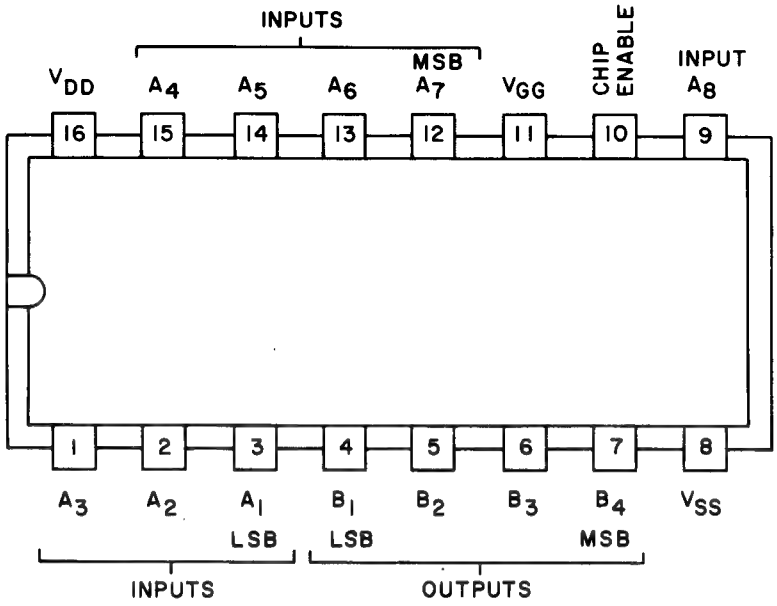

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Figure 72. 256-4 (1024) Bit Static ROM (138C061H03, 138C061G01) (Sheet 1 of 5)

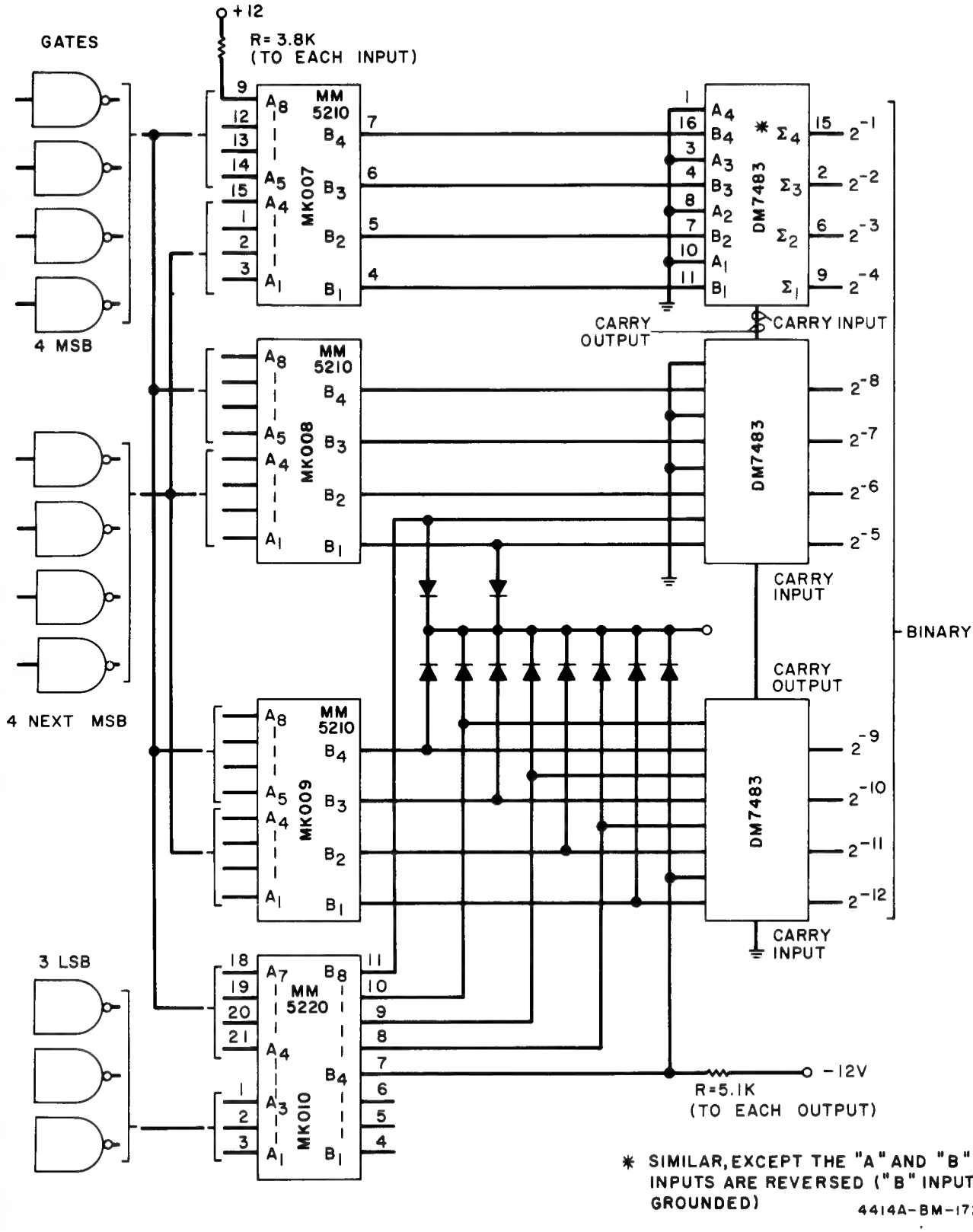

Figure 72. 256-4 (1024) Bit Static ROM (138C061H03, 138C061G01)
(Sheet 2 of 5)

This device is a sine function generator containing four 1024-bit ROM's. MK007, MK008, MK009, and MK010 are the 1024-bit static read-only memories. They are P-channel enhancement mode monolithic MOS integrated circuits utilizing low threshold voltage technology. MK007, MK008, and MK009 are non-volatile memories organized as 256-4 bit words. MK010 is a non-volatile memory organized as 128-8 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication. DM7483 is a 4-bit binary full adder. The table in figure 72 defines the address-output code for MK007. The table in figure 73 is for MK008, figure 74 is for MK009, and figure 75 is for MK010. MK007, MK008, and MK009 each have eight inputs that define the address. The address on the table which is in decimal corresponds to the memory input which is eight binary digits (A1 to A8). The table shows the output code (B1, B2, B3, B4) that will be present when the input (A1 to A8) is the same as the address. For MK007, an address of zero (A1 = 0, A2 = 0, A3 = 0, A4 = 0, A5 = 0, A6 = 0, A7 = 0, A8 = 0) will have an output of B1 = 1, B2 = 1, B3 = 1, and B4 = 1. An address of one (A1 = 0, A2 = 0, A3 = 0, A4 = 0, A5 = 0, A6 = 0, A7 = 0, A8 = 1) will have an output of B1 = 1, B2 = 1, B3 = 1, and B4 = 1. The address-output code table for MK008 and MK009 is read the same way one reads the table for MK007. The table for MK010 is read like the MK007 table except the address which is in decimal corresponds to the memory input which is seven binary digits (A1 to A7) and the output code for MK010 has eight digits (B1 to B8).

Figure 72. 256-4 (1024) Bit Static ROM (138C061H03-138C061G01)
(Sheet 3 of 5)

Address	Output Code			
	B4	B3	B2	B1
0	1	1	1	1
1	1	1	1	1
2	1	1	1	1
3	1	1	1	1
4	1	1	1	1
5	1	1	1	1
6	1	1	1	1
7	1	1	1	1
8	1	1	1	1
9	1	1	1	1
10	1	1	1	1
11	1	1	1	0
12	1	1	1	0
13	1	1	1	0
14	1	1	1	0
15	1	1	1	0
16	1	1	1	0
17	1	1	1	0
18	1	1	1	0
19	1	1	1	0
20	1	1	1	0
21	1	1	0	1
22	1	1	0	1
23	1	1	0	1
24	1	1	0	1
25	1	1	0	1
26	1	1	0	1
27	1	1	0	1
28	1	1	0	1
29	1	1	0	1
30	1	1	0	1
31	1	1	0	0
32	1	1	0	0
33	1	1	0	0
34	1	1	0	0
35	1	1	0	0
36	1	1	0	0
37	1	1	0	0
38	1	1	0	0
39	1	1	0	0
40	1	1	0	0
41	1	1	0	0

Address	Output Code			
	B4	B3	B2	B1
42	1	0	1	1
43	1	0	1	1
44	1	0	1	1
45	1	0	1	1
46	1	0	1	1
47	1	0	1	1
48	1	0	1	1
49	1	0	1	1
50	1	0	1	1
51	1	0	1	1
52	1	0	1	0
53	1	0	1	0
54	1	0	1	0
55	1	0	1	0
56	1	0	1	0
57	1	0	1	0
58	1	0	1	0
59	1	0	1	0
60	1	0	1	0
61	1	0	1	0
62	1	0	1	0
63	1	0	0	1
64	1	0	0	1
65	1	0	0	1
66	1	0	0	1
67	1	0	0	1
68	1	0	0	1
69	1	0	0	1
70	1	0	0	1
71	1	0	0	1
72	1	0	0	1
73	1	0	0	1
74	1	0	0	0
75	1	0	0	0
76	1	0	0	0
77	1	0	0	0
78	1	0	0	0
79	1	0	0	0
80	1	0	0	0
81	1	0	0	0
82	1	0	0	0
83	1	0	0	0

Address	Output Code			
	B4	B3	B2	B1
84	1	0	0	0
85	1	0	0	0
86	0	1	1	1
87	0	1	1	1
88	0	1	1	1
89	0	1	1	1
90	0	1	1	1
91	0	1	1	1
92	0	1	1	1
93	0	1	1	1
94	0	1	1	1
95	0	1	1	1
96	0	1	1	1
97	0	1	1	1
98	0	1	1	0
99	0	1	1	0
100	0	1	1	0
101	0	1	1	0
102	0	1	1	0
103	0	1	1	0
104	0	1	1	0
105	0	1	1	0
106	0	1	1	0
107	0	1	1	0
108	0	1	1	0
109	0	1	1	0
110	0	1	1	0
111	0	1	0	1
112	0	1	0	1
113	0	1	0	1
114	0	1	0	1
115	0	1	0	1
116	0	1	0	1
117	0	1	0	1
118	0	1	0	1
119	0	1	0	1
120	0	1	0	1
121	0	1	0	1
122	0	1	0	1
123	0	1	0	1
124	0	1	0	0
125	0	1	0	0

Address	Output Code			
	B4	B3	B2	B1
126	0	1	0	0
127	0	1	0	0
128	0	1	0	0
129	0	1	0	0
130	0	1	0	0
131	0	1	0	0
132	0	1	0	0
133	0	1	0	0
134	0	1	0	0
135	0	1	0	0
136	0	1	0	0
137	0	1	0	0
138	0	1	0	0
139	0	0	1	1
140	0	0	1	1
141	0	0	1	1
142	0	0	1	1
143	0	0	1	1
144	0	0	1	1
145	0	0	1	1
146	0	0	1	1
147	0	0	1	1
148	0	0	1	1
149	0	0	1	1
150	0	0	1	1
151	0	0	1	1
152	0	0	1	1
153	0	0	1	1
154	0	0	1	1
155	0	0	1	0
156	0	0	1	0
157	0	0	1	0
158	0	0	1	0
159	0	0	1	0
160	0	0	1	0
161	0	0	1	0
162	0	0	1	0
163	0	0	1	0
164	0	0	1	0
165	0	0	1	0
166	0	0	1	0
167	0	0	1	0

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Figure 72. 256-4 (1024) Bit Static ROM (138C061H03, 138C061G01) (Sheet 4 of 5)

Address	Output Code			
	B4	B3	B2	B1
168	0	0	1	0
169	0	0	1	0
170	0	0	1	0
171	0	0	1	0
172	0	0	1	0
173	0	0	1	0
174	0	0	0	1
175	0	0	0	1
176	0	0	0	1
177	0	0	0	1
178	0	0	0	1
179	0	0	0	1
180	0	0	0	1
181	0	0	0	1
182	0	0	0	1
183	0	0	0	1
184	0	0	0	1
185	0	0	0	1
186	0	0	0	1
187	0	0	0	1
188	0	0	0	1
189	0	0	0	1
190	0	0	0	1
191	0	0	0	1
192	0	0	0	1
193	0	0	0	1
194	0	0	0	1
195	0	0	0	1
196	0	0	0	1
197	0	0	0	1
198	0	0	0	1
199	0	0	0	0
200	0	0	0	0
201	0	0	0	0
202	0	0	0	0
203	0	0	0	0
204	0	0	0	0
205	0	0	0	0
206	0	0	0	0
207	0	0	0	0
208	0	0	0	0
209	0	0	0	0

Address	Output Code			
	B4	B3	B2	B1
210	0	0	0	0
211	0	0	0	0
212	0	0	0	0
213	0	0	0	0
214	0	0	0	0
215	0	0	0	0
216	0	0	0	0
217	0	0	0	0
218	0	0	0	0
219	0	0	0	0
220	0	0	0	0
221	0	0	0	0
222	0	0	0	0
223	0	0	0	0
224	0	0	0	0
225	0	0	0	0
226	0	0	0	0
227	0	0	0	0
228	0	0	0	0
229	0	0	0	0
230	0	0	0	0
231	0	0	0	0
232	0	0	0	0
233	0	0	0	0
234	0	0	0	0
235	0	0	0	0
236	0	0	0	0
237	0	0	0	0
238	0	0	0	0
239	0	0	0	0
240	0	0	0	0
241	0	0	0	0
242	0	0	0	0
243	0	0	0	0
244	0	0	0	0
245	0	0	0	0
246	0	0	0	0
247	0	0	0	0
248	0	0	0	0
249	0	0	0	0
250	0	0	0	0
251	0	0	0	0

Address	Output Code			
	B4	B3	B2	B1
252	0	0	0	0
253	0	0	0	0
254	0	0	0	0
255	0	0	0	0

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Figure 72. 256-4 (1024) Bit Static ROM (138C061H03, 138C061G01) (Sheet 5 of 5)

Address	Output Data			
	B4	B3	B2	B1
0	1	1	1	1
1	1	1	1	0
2	1	1	0	0
3	1	0	1	1
4	1	0	0	1
5	1	0	0	0
6	0	1	1	0
7	0	1	0	0
8	0	0	1	1
9	0	0	0	1
10	0	0	0	0
11	1	1	1	0
12	1	1	0	1
13	1	0	1	1
14	1	0	1	0
15	1	0	0	0
16	0	1	1	0
17	0	1	0	1
18	0	0	1	1
19	0	0	1	0
20	0	0	0	0
21	1	1	1	1
22	1	1	0	1
23	1	0	1	1
24	1	0	1	0
25	1	0	0	0
26	0	1	1	1
27	0	1	0	1
28	0	1	0	0
29	0	0	1	0
30	0	0	0	1
31	1	1	1	1
32	1	1	1	0
33	1	1	0	0
34	1	0	1	0
35	1	0	0	1
36	0	1	1	1
37	0	1	1	0
38	0	1	0	0
39	0	0	1	1
40	0	0	0	1
41	0	0	0	0

Address	Output Data			
	B4	B3	B2	B1
42	1	1	1	0
43	1	1	0	1
44	1	0	1	1
45	1	0	1	0
46	1	0	0	0
47	0	1	1	1
48	0	1	0	1
49	0	1	0	0
50	0	0	1	0
51	0	0	0	1
52	1	1	1	1
53	1	1	1	0
54	1	1	0	0
55	1	0	1	1
56	1	0	0	1
57	1	0	0	0
58	0	1	1	0
59	0	1	0	1
60	0	0	1	1
61	0	0	1	0
62	0	0	0	0
63	1	1	1	1
64	1	1	1	0
65	1	1	0	0
66	1	0	1	1
67	1	0	0	1
68	1	0	0	0
69	0	1	1	0
70	0	1	0	1
71	0	0	1	1
72	0	0	1	0
73	0	0	0	1
74	1	1	1	1
75	1	1	1	0
76	1	1	0	0
77	1	0	1	1
78	1	0	1	0
79	1	0	0	0
80	0	1	1	1
81	0	1	0	1
82	0	1	1	1
83	0	0	1	1

Address	Output Data			
	B4	B3	B2	B1
84	0	0	0	1
85	0	0	0	0
86	1	1	1	1
87	1	1	0	1
88	1	1	0	0
89	1	0	1	1
90	1	0	0	1
91	1	0	0	0
92	0	1	1	1
93	0	1	0	1
94	0	1	0	0
95	0	0	1	1
96	0	0	0	1
97	0	0	0	0
98	1	1	1	1
99	1	1	0	1
100	1	1	0	0
101	1	0	1	1
102	1	0	1	0
103	1	0	0	0
104	0	1	1	1
105	0	1	1	0
106	0	1	0	0
107	0	0	1	1
108	0	0	1	0
109	0	0	0	1
110	0	0	0	0
111	1	1	1	0
112	1	1	0	1
113	1	1	0	0
114	1	0	1	1
115	1	0	0	1
116	1	0	0	0
117	0	1	1	1
118	0	1	1	0
119	0	1	0	1
120	0	1	0	0
121	0	0	1	0
122	0	0	0	1
123	0	0	0	0
124	1	1	1	1
125	1	1	1	0

Address	Output Data			
	B4	B3	B2	B1
126	1	1	0	1
127	1	1	0	0
128	1	0	1	0
129	1	0	0	1
130	1	0	0	0
131	0	1	1	1
132	0	1	1	0
133	0	1	0	1
134	0	1	0	0
135	0	0	1	1
136	0	0	1	0
137	0	0	0	1
138	0	0	0	0
139	1	1	1	1
140	1	1	1	0
141	1	1	0	1
142	1	1	0	0
143	1	0	1	1
144	1	0	1	0
145	1	0	0	1
146	1	0	0	0
147	0	1	1	1
148	0	1	1	0
149	0	1	0	1
150	0	1	0	0
151	0	0	1	1
152	0	0	1	0
153	0	0	0	1
154	0	0	0	0
155	1	1	1	1
156	1	1	1	0
157	1	1	0	1
158	1	1	0	0
159	1	0	1	1
160	1	0	1	1
161	1	0	1	0
162	1	0	0	1
163	1	0	0	0
164	0	1	1	1
165	0	1	1	0
166	0	1	1	0
167	0	1	0	1

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Figure 73. 256-4 (1024) Bit Static ROM (138C061H04, 138C061G01) (Sheet 1 of 2)

Address	Output Data			
	B4	B3	B2	B1
168	0	1	0	0
169	0	0	1	1
170	0	0	1	0
171	0	0	1	0
172	0	0	0	1
173	0	0	0	0
174	1	1	1	1
175	1	1	1	0
176	1	1	1	0
177	1	1	0	1
178	1	1	0	0
179	1	1	0	0
180	1	0	1	1
181	1	0	1	0
182	1	0	0	1
183	1	0	0	1
184	1	0	0	0
185	0	1	1	1
186	0	1	1	1
187	0	1	1	0
188	0	1	0	1
189	0	1	0	1
190	0	1	0	0
191	0	1	0	0
192	0	0	1	1
193	0	0	1	0
194	0	0	1	0
195	0	0	0	1
196	0	0	0	1
197	0	0	0	0
198	0	0	0	0
199	1	1	1	1
200	1	1	1	0
201	1	1	1	0
202	1	1	0	1
203	1	1	0	1
204	1	1	0	0
205	1	1	0	0
206	1	0	1	1
207	1	0	1	1
208	1	0	1	0
209	1	0	1	0

Address	Output Data			
	B4	B3	B2	B1
210	1	0	1	0
211	1	0	0	1
212	1	0	0	1
213	1	0	0	0
214	1	0	0	0
215	1	0	0	0
216	0	1	1	1
217	0	1	1	1
218	0	1	1	0
219	0	1	1	0
220	0	1	1	0
221	0	1	0	1
222	0	1	0	1
223	0	1	0	1
224	0	1	0	0
225	0	1	0	0
226	0	1	0	0
227	0	1	0	0
228	0	0	1	1
229	0	0	1	1
230	0	0	1	1
231	0	0	1	0
232	0	0	1	0
233	0	0	1	0
234	0	0	1	0
235	0	0	1	0
236	0	0	0	1
237	0	0	0	1
238	0	0	0	1
239	0	0	0	1
240	0	0	0	1
241	0	0	0	1
242	0	0	0	0
243	0	0	0	0
244	0	0	0	0
245	0	0	0	0
246	0	0	0	0
247	0	0	0	0
248	0	0	0	0
249	0	0	0	0
250	0	0	0	0
251	0	0	0	0

Address	Output Data			
	B4	B3	B2	B1
252	0	0	0	0
253	0	0	0	0
254	0	0	0	0
255	0	0	0	0

NOTE: SEE FIGURE 72 FOR CONNECTION AND INTERFACE LOGIC DIAGRAM

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Figure 73. 256-4 (1024) Bit Static ROM (138C061H04, 138C061G01) (Sheet 2 of 2)

Address	Output Code			
	B4	B3	B2	B1
0	1	1	1	1
1	0	1	1	0
2	1	1	0	1
3	0	1	0	0
4	1	0	1	0
5	0	0	0	1
6	1	0	0	0
7	1	1	1	1
8	0	1	1	0
9	1	1	0	1
10	0	1	0	0
11	1	0	1	1
12	0	0	1	0
13	1	0	0	1
14	0	0	0	0
15	0	1	1	1
16	1	1	1	0
17	0	1	0	1
18	1	1	0	0
19	0	0	1	1
20	1	0	1	0
21	0	0	0	1
22	1	0	0	0
23	1	1	1	1
24	0	1	1	0
25	1	1	0	1
26	0	1	0	0
27	1	1	0	0
28	0	0	1	1
29	1	0	1	0
30	0	0	0	1
31	1	0	0	1
32	0	0	0	0
33	0	1	1	1
34	1	1	1	1
35	0	1	1	0
36	1	1	1	0
37	0	1	0	1
38	1	1	0	1
39	0	1	0	0
40	1	1	0	1
41	0	0	1	1

Address	Output Code			
	B4	B3	B2	B1
42	1	0	1	1
43	0	0	1	1
44	1	0	1	1
45	0	0	1	0
46	1	0	1	0
47	0	0	1	0
48	1	0	1	0
49	0	0	1	0
50	1	0	1	0
51	0	0	1	0
52	1	0	1	0
53	0	0	1	0
54	1	0	1	1
55	0	0	1	1
56	1	0	1	1
57	0	0	1	1
58	1	1	0	0
59	0	1	0	0
60	1	1	0	1
61	0	1	0	1
62	1	1	1	0
63	0	1	1	1
64	0	0	0	0
65	1	0	0	0
66	0	0	0	1
67	1	0	1	0
68	0	0	1	1
69	1	1	0	0
70	0	1	0	1
71	1	1	1	1
72	1	0	0	0
73	0	0	0	1
74	1	0	1	0
75	0	1	0	0
76	1	1	0	1
77	0	1	1	1
78	0	0	0	1
79	1	0	1	0
80	0	1	0	0
81	1	1	1	0
82	1	0	0	0
83	0	0	1	0

Address	Output Code			
	B4	B3	B2	B1
84	1	1	0	0
85	0	1	1	0
86	0	0	0	1
87	1	0	1	1
88	0	1	0	1
89	0	0	0	0
90	1	0	1	0
91	0	1	0	1
92	0	0	0	0
93	1	0	1	0
94	0	1	0	1
95	0	0	0	0
96	1	0	1	1
97	0	1	1	1
98	0	0	1	0
99	1	1	0	1
100	1	0	0	1
101	0	1	0	0
102	0	0	0	0
103	1	0	1	1
104	0	1	1	1
105	0	0	1	1
106	1	1	1	1
107	1	0	1	1
108	0	1	1	1
109	0	0	1	1
110	0	0	0	0
111	1	1	0	0
112	1	0	0	1
113	0	1	0	1
114	0	0	1	0
115	1	1	1	1
116	1	1	0	0
117	1	0	0	1
118	0	1	1	0
119	0	0	1	1
120	0	0	0	0
121	1	1	1	0
122	1	0	1	1
123	1	0	0	1
124	0	1	1	1
125	0	1	0	0

Address	Output Code			
	B4	B3	B2	B1
126	0	0	1	0
127	0	0	0	1
128	1	1	1	1
129	1	1	0	1
130	1	0	1	1
131	1	0	1	0
132	1	0	0	1
133	0	1	1	1
134	0	1	1	0
135	0	1	0	1
136	0	1	0	0
137	0	0	1	1
138	0	0	1	1
139	0	0	1	0
140	0	0	1	0
141	0	0	0	1
142	0	0	0	1
143	0	0	0	1
144	0	0	0	1
145	0	0	0	1
146	0	0	0	1
147	0	0	1	0
148	0	0	1	0
149	0	0	1	1
150	0	0	1	1
151	0	1	0	0
152	0	1	0	1
153	0	1	1	0
154	0	1	1	1
155	1	0	0	1
156	1	0	1	0
157	1	1	0	0
158	1	1	1	0
159	1	1	1	1
160	0	0	0	1
161	0	0	1	1
162	0	1	1	0
163	1	0	0	0
164	1	0	1	1
165	1	1	0	1
166	0	0	0	0
167	0	0	1	1

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Figure 74. 256-4 (1024) Bit Static ROM (138C061H05, 138C061G01) (Sheet 1 of 2)

Address	Output Code			
	B4	B3	B2	B1
168	0	1	1	0
169	1	0	0	1
170	1	1	0	0
171	0	0	0	0
172	0	0	1	1
173	0	1	1	1
174	1	0	1	1
175	1	1	1	1
176	0	0	1	1
177	0	1	1	1
178	1	0	1	1
179	0	0	0	0
180	0	1	0	0
181	1	0	0	1
182	1	1	1	0
183	0	0	1	1
184	1	0	0	0
185	1	1	1	0
186	0	0	1	1
187	1	0	0	1
188	1	1	1	0
189	0	1	0	0
190	1	0	1	0
191	0	0	0	1
192	0	1	1	1
193	1	1	0	1
194	0	1	0	0
195	1	0	1	1
196	0	0	0	1
197	1	0	0	1
198	0	0	0	0
199	0	1	1	1
200	1	1	1	0
201	0	1	1	0
202	1	1	1	0
203	0	1	1	0
204	1	1	1	0
205	0	1	1	0
206	1	1	1	0
207	0	1	1	1
208	1	1	1	1
209	1	0	0	0

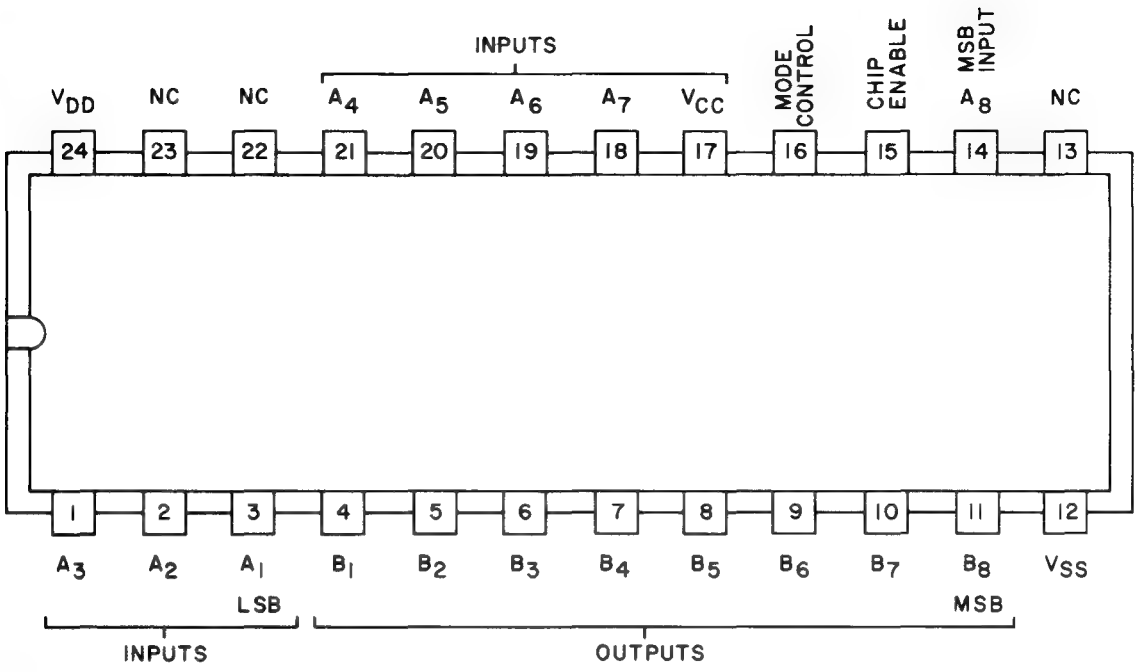
Address	Output Code			
	B4	B3	B2	B1
210	0	0	0	1
211	1	1	1	0
212	0	0	1	1
213	1	1	0	1
214	0	1	1	0
215	0	0	0	0
216	1	0	1	0
217	0	1	0	0
218	1	1	1	0
219	1	0	0	0
220	0	0	1	1
221	1	1	0	1
222	1	0	0	0
223	1	0	0	0
224	1	1	1	0
225	1	0	0	1
226	0	1	0	0
227	0	0	0	0
228	1	0	1	1
229	0	1	1	1
230	0	0	1	1
231	1	1	1	1
232	1	0	1	1
233	1	0	0	0
234	0	1	0	0
235	0	0	0	1
236	1	1	1	0
237	1	0	1	1
238	1	0	0	0
239	0	1	0	1
240	0	0	1	1
241	0	0	0	0
242	1	1	1	0
243	1	1	0	0
244	1	0	1	0
245	1	0	0	0
246	0	1	1	1
247	0	1	0	1
248	0	1	0	0
249	0	0	1	1
250	0	0	1	0
251	0	0	0	1

Address	Output Code			
	B4	B3	B2	B1
252	0	0	0	0
253	0	0	0	0
254	0	0	0	0
255	0	0	0	0

NOTE: SEE FIGURE 72 FOR CONNECTION AND INTERFACE LOGIC DIAGRAM

4414A-BM-195A

Figure 74. 256-4 (1024) Bit Static ROM (138C061H05, 138C061G01) (Sheet 2 of 2)



NOTE:

NC = NO CONNECTION

SEE FIGURE 72 FOR
INTERFACE LOGIC DIAGRAM

4414A-BM-196A

Figure 75. 128-8(1024) Bit Static ROM (138C061H06, 138C061G01)
(Sheet 1 of 2)

ADDRESS	OUTPUT CODE							
	B8	B7	B6	B5	B4	B3	B2	B1
0	1	1	1	1	1	X	X	X
1	1	1	1	0	0	X	X	X
2	1	1	0	0	1	X	X	X
3	1	0	1	1	0	X	X	X
4	1	0	0	1	0	X	X	X
5	0	1	1	1	1	X	X	X
6	0	1	1	0	0	X	X	X
7	0	1	0	0	1	X	X	X
8	1	1	1	1	1	X	X	X
9	1	1	1	0	0	X	X	X
10	1	1	0	0	1	X	X	X
11	1	0	1	1	0	X	X	X
12	1	0	0	1	1	X	X	X
13	0	1	1	1	1	X	X	X
14	0	1	1	0	0	X	X	X
15	0	1	0	0	1	X	X	X
16	1	1	1	1	1	X	X	X
17	1	1	1	0	0	X	X	X
18	1	1	0	0	1	X	X	X
19	1	0	1	1	0	X	X	X
20	1	0	0	1	1	X	X	X
21	1	0	0	0	0	X	X	X
22	0	1	1	0	1	X	X	X
23	0	1	0	1	0	X	X	X
24	1	1	1	1	1	X	X	X
25	1	1	1	0	0	X	X	X
26	1	1	0	0	1	X	X	X
27	1	0	1	1	0	X	X	X
28	1	0	0	1	1	X	X	X
29	1	0	0	0	0	X	X	X
30	0	1	1	0	1	X	X	X
31	0	1	0	1	0	X	X	X
32	1	1	1	1	1	X	X	X
33	1	1	1	0	0	X	X	X
34	1	1	0	0	1	X	X	X
35	1	0	1	1	0	X	X	X
36	1	0	1	0	0	X	X	X
37	1	0	0	0	1	X	X	X
38	0	1	1	1	0	X	X	X
39	0	1	0	1	1	X	X	X
40	1	1	1	1	1	X	X	X
41	1	1	1	0	0	X	X	X
42	1	1	0	1	0	X	X	X

ADDRESS	OUTPUT CODE							
	B8	B7	B6	B5	B4	B3	B2	B1
43	1	0	1	1	1	X	X	X
44	1	0	1	0	0	X	X	X
45	1	0	0	1	0	X	X	X
46	0	1	1	1	1	X	X	X
47	0	1	1	0	0	X	X	X
48	1	1	1	1	1	X	X	X
49	1	1	1	0	0	X	X	X
50	1	1	0	1	0	X	X	X
51	1	0	1	1	1	X	X	X
52	1	0	1	0	1	X	X	X
53	1	0	0	1	0	X	X	X
54	1	0	0	0	0	X	X	X
55	0	1	1	0	1	X	X	X
56	1	1	1	1	1	X	X	X
57	1	1	1	0	1	X	X	X
58	1	1	0	1	0	X	X	X
59	1	1	0	0	0	X	X	X
60	1	0	1	1	0	X	X	X
61	1	0	0	1	1	X	X	X
62	1	0	0	0	1	X	X	X
63	0	1	1	1	1	X	X	X
64	1	1	1	1	1	X	X	X
65	1	1	1	0	1	X	X	X
66	1	1	0	1	1	X	X	X
67	1	1	0	0	1	X	X	X
68	1	0	1	1	1	X	X	X
69	1	0	1	0	1	X	X	X
70	1	0	0	1	0	X	X	X
71	1	0	0	0	0	X	X	X
72	1	1	1	1	1	X	X	X
73	1	1	1	0	1	X	X	X
74	1	1	0	1	1	X	X	X
75	1	1	0	0	1	X	X	X
76	1	1	0	0	0	X	X	X
77	1	0	1	1	0	X	X	X
78	1	0	1	0	0	X	X	X
79	1	0	0	1	0	X	X	X
80	1	1	1	1	1	X	X	X
81	1	1	1	0	1	X	X	X
82	1	1	1	0	0	X	X	X
83	1	1	0	1	0	X	X	X
84	1	1	0	0	1	X	X	X
85	1	0	1	1	1	X	X	X

ADDRESS	OUTPUT CODE							
	B8	B7	B6	B5	B4	B3	B2	B1
86	1	0	1	0	1	X	X	X
87	1	0	1	0	0	X	X	X
88	1	1	1	1	1	X	X	X
89	1	1	1	1	0	X	X	X
90	1	1	1	0	0	X	X	X
91	1	1	0	1	1	X		X
92	1	1	0	1	0	X	X	X
93	1	1	0	0	0	X	X	X
94	1	0	1	1	1	X	X	X
95	1	0	1	1	0	X	X	X
96	1	1	1	1	1	X	X	X
97	1	1	1	1	0	X	X	X
98	1	1	1	0	1	X	X	X
99	1	1	1	0	0	X	X	X
100	1	1	0	1	1	X	X	X
101	1	1	0	1	0	X	X	X
102	1	1	0	0	1	X	X	X
103	1	1	0	0	0	X	X	X
104	1	1	1	1	1	X	X	X
105	1	1	1	1	0	X	X	X
106	1	1	1	0	1	X	X	X
107	1	1	1	0	1	X	X	X
108	1	1	1	0	0	X	X	X
109	1	1	0	1	1	X	X	X
110	1	1	0	1	0	X	X	X
111	1	1	0	1	0	X	X	X
112	1	1	1	1	1	X	X	X
113	1	1	1	1	1	X	X	X
114	1	1	1	1	0	X	X	X
115	1	1	1	1	0	X	X	X
116	1	1	1	0	1	X	X	X
117	1	1	1	0	1	X	X	X
118	1	1	1	0	0	X	X	X
119	1	1	1	0	0	X	X	X
120	1	1	1	1	1	X	X	X
121	1	1	1	1	1	X	X	X
122	1	1	1	1	1	X	X	X
123	1	1	1	1	1	X	X	X
124	1	1	1	1	1	X	X	X
125	1	1	1	1	1	X	X	X
126	1	1	1	1	1	X	X	X
127	1	1	1	1	1	X	X	X

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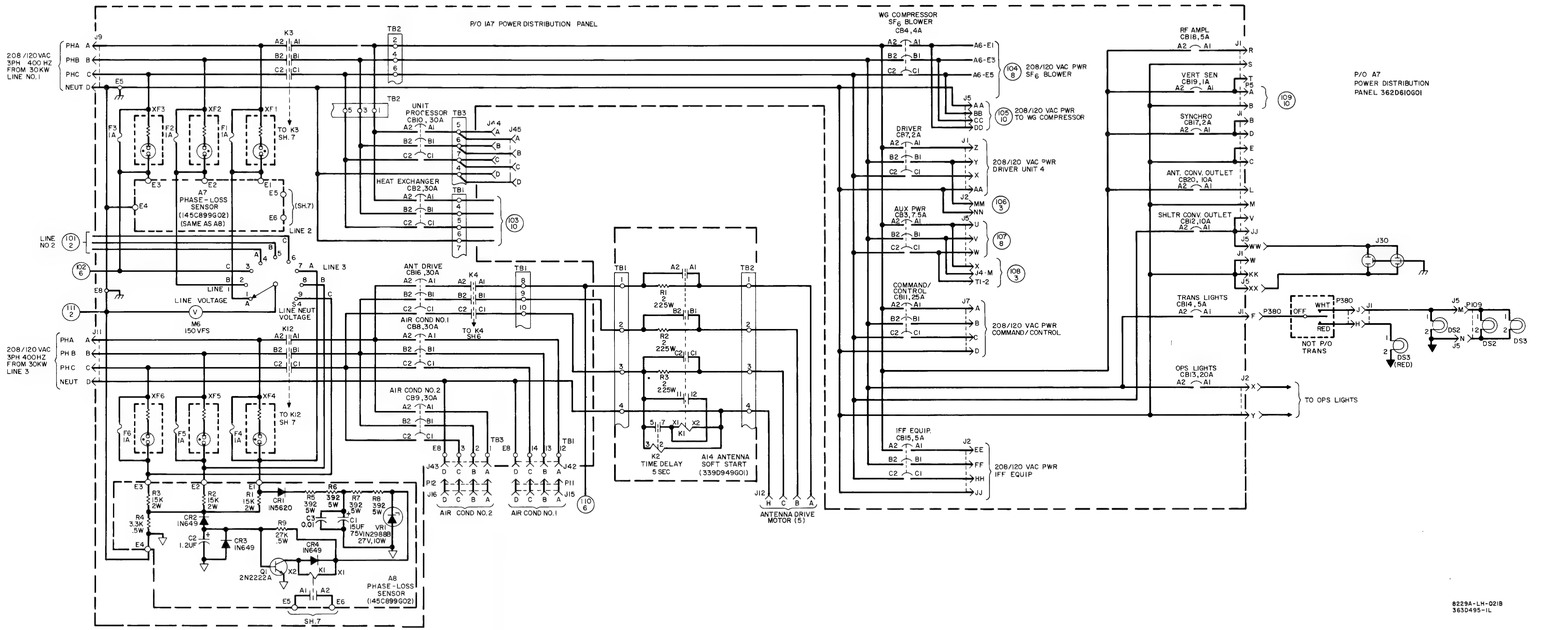
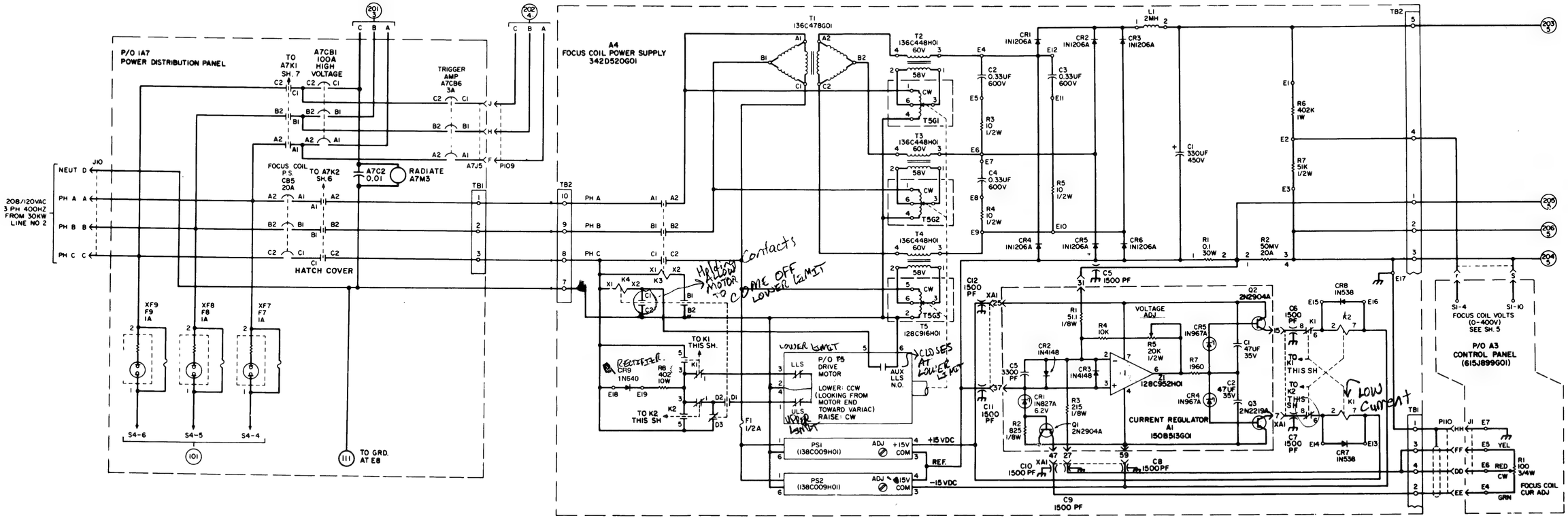
Figure 75. 128-8 (1024) Bit Static ROM (138C061H06, 138C061G01) (Sheet 2 of 2)

GPO 587-000/21277

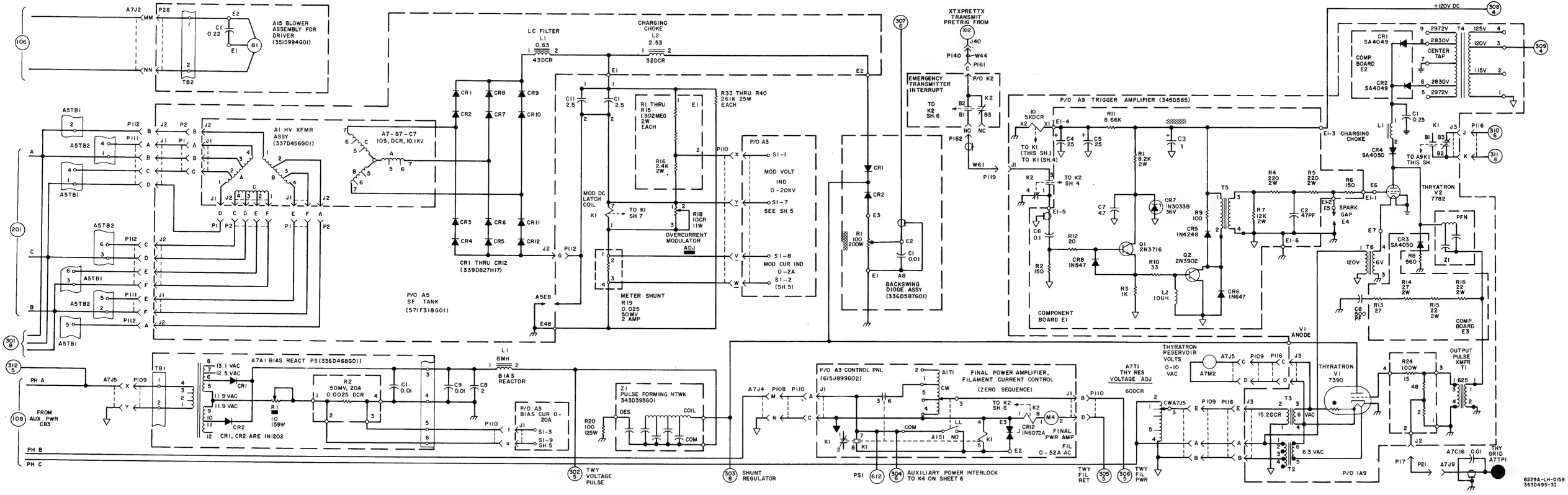


Change 7 FO-36. Ⓐ Ⓒ Ⓓ Transmitter (615J745) Schematic Diagram (Sheet 1 of 12)

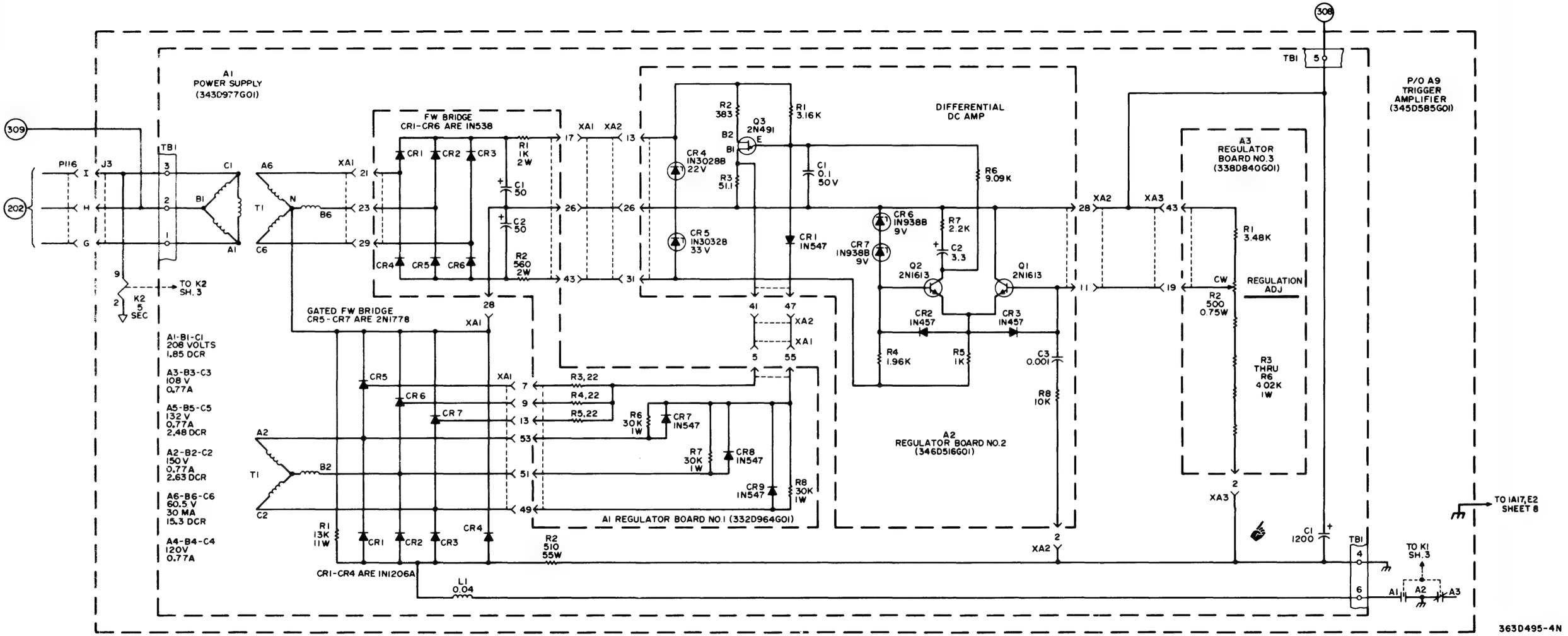


Change 10

FO-36. Ⓐ Ⓘ Ⓝ Transmitter (615J745) Schematic Diagram (Sheet 2 of 12)

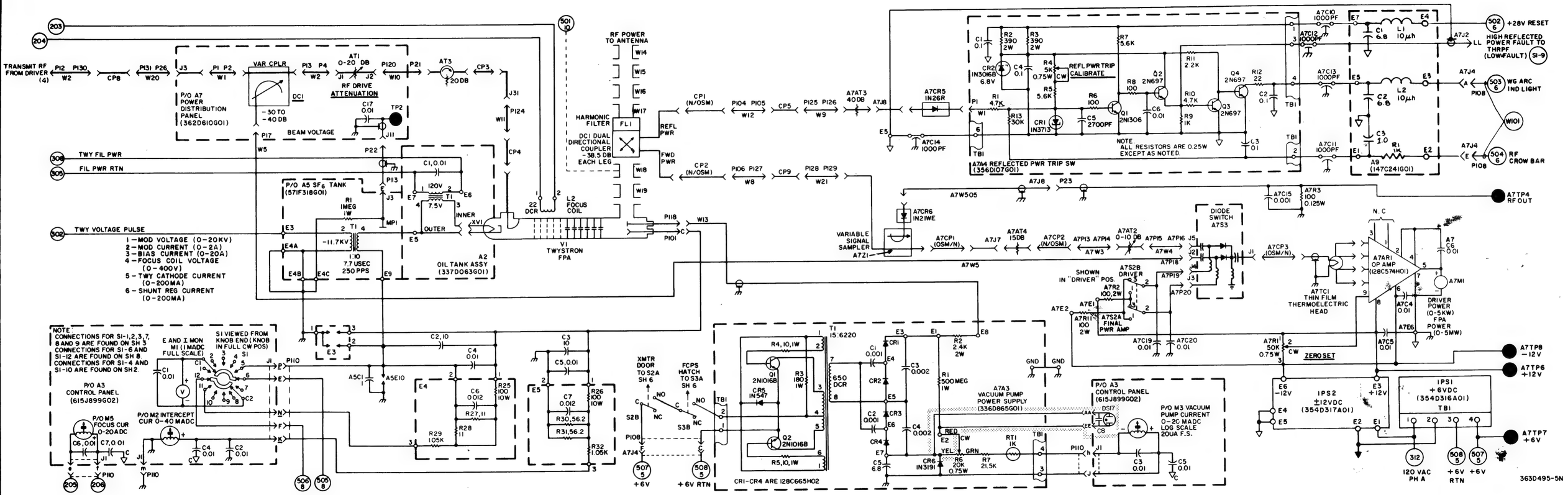


Change 8 FO-36. Ⓗ Ⓘ Ⓝ Transmitter (615J745) Schematic Diagram (Sheet 3 of 12)



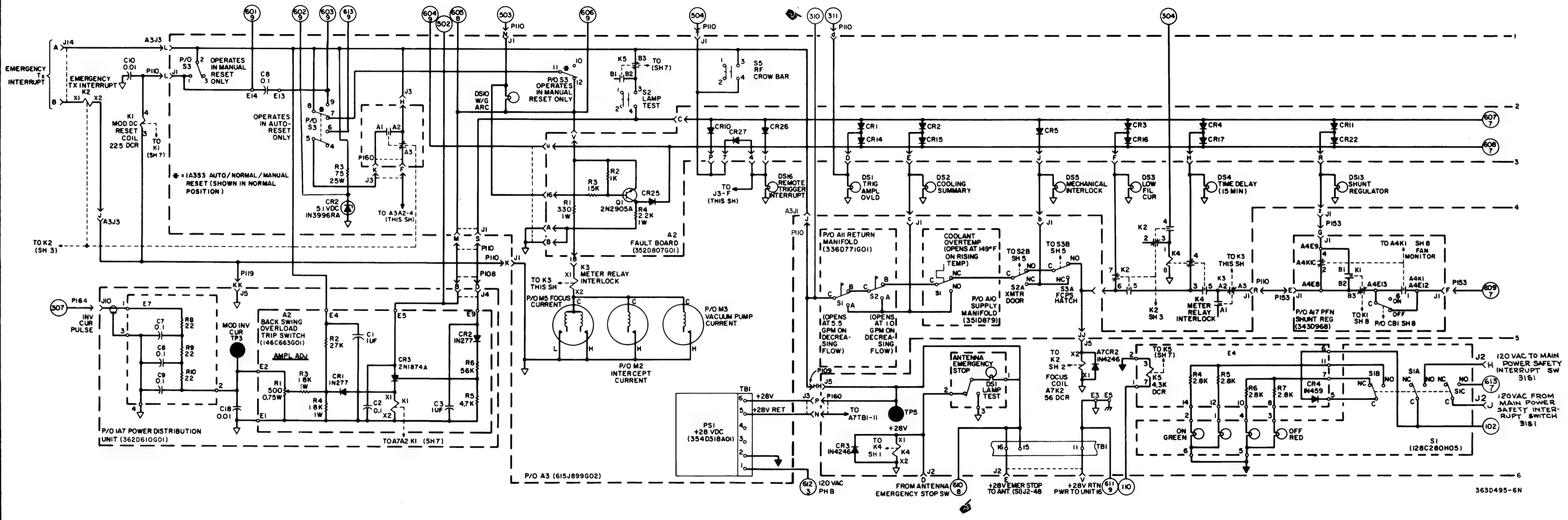
Change 10

FO-36. (H) (T) (N) Transmitter (615J745) Schematic Diagram (Sheet 4 of 12)



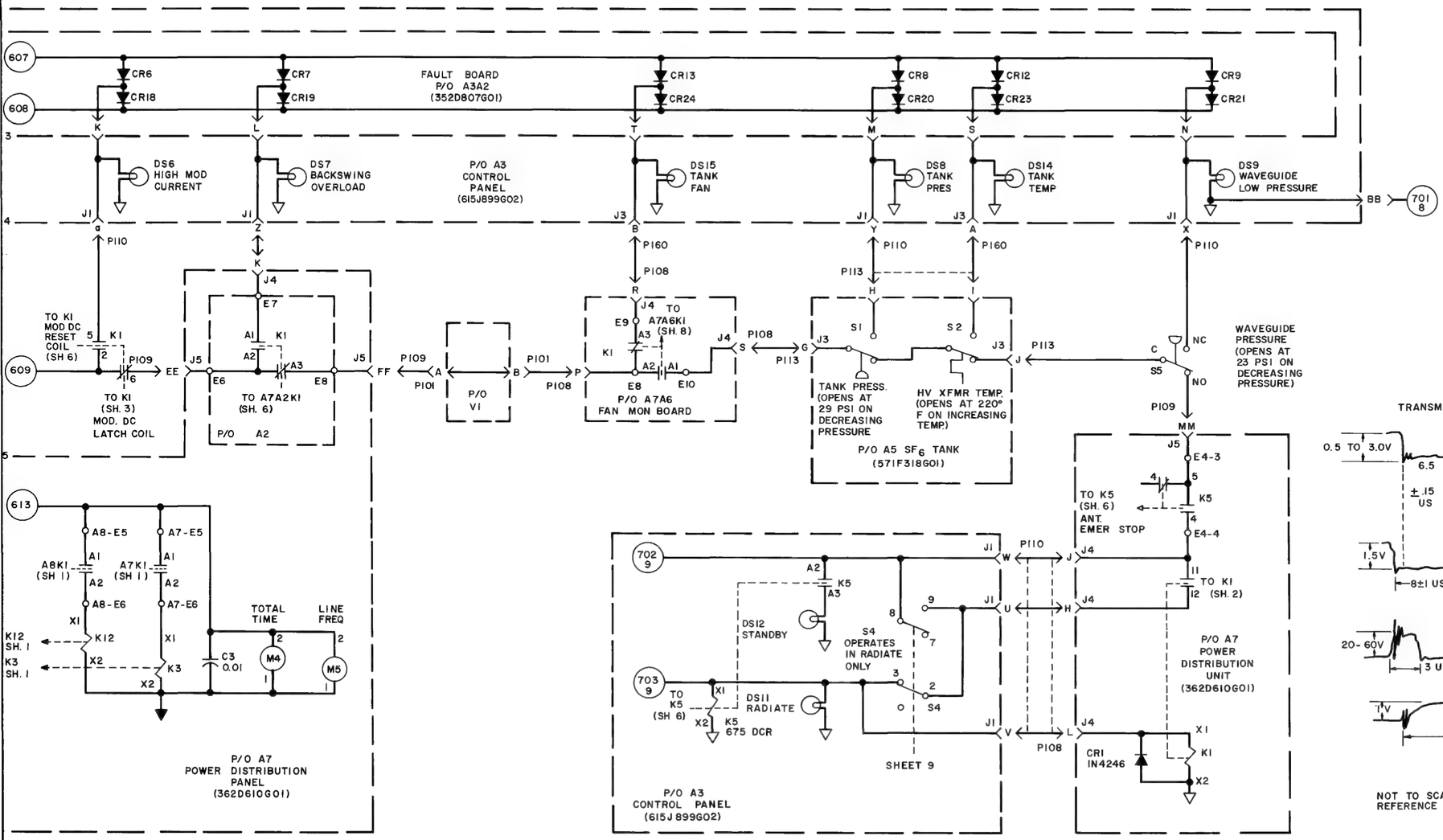
Change 10

FO-36. Ⓗ Ⓘ Ⓝ Transmitter (615J745) Schematic Diagram (Sheet 5 of 12)



Change 10

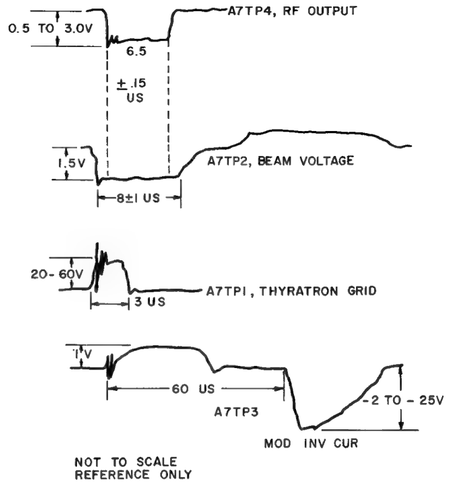
FO-36. (B) (I) (N) Transmitter (615J745) Schematic Diagram (Sheet 6 of 12)



HEAT EXCHANGER A6A1
WIRE LIST

FROM	WIRE	TO
J1-A	300	K1-A1
B	301	B1
C	302	C1
D	100	X2
P2-A	303	K1-A2
B	304	B2
C	305	C2
D	107	C1
E	104	K2-10
M1-1	109	K1-X2
2	110	X1
K1-X1	112	S4-NC
S4-C	111	S5-NC
S5-C	103	K2-6
K1-X2	101	7
K2-6	102	8
8	105	S3-1
S3-1	106	K1-C1
2	108	K2-9

TRANSMITTER WAVEFORMS

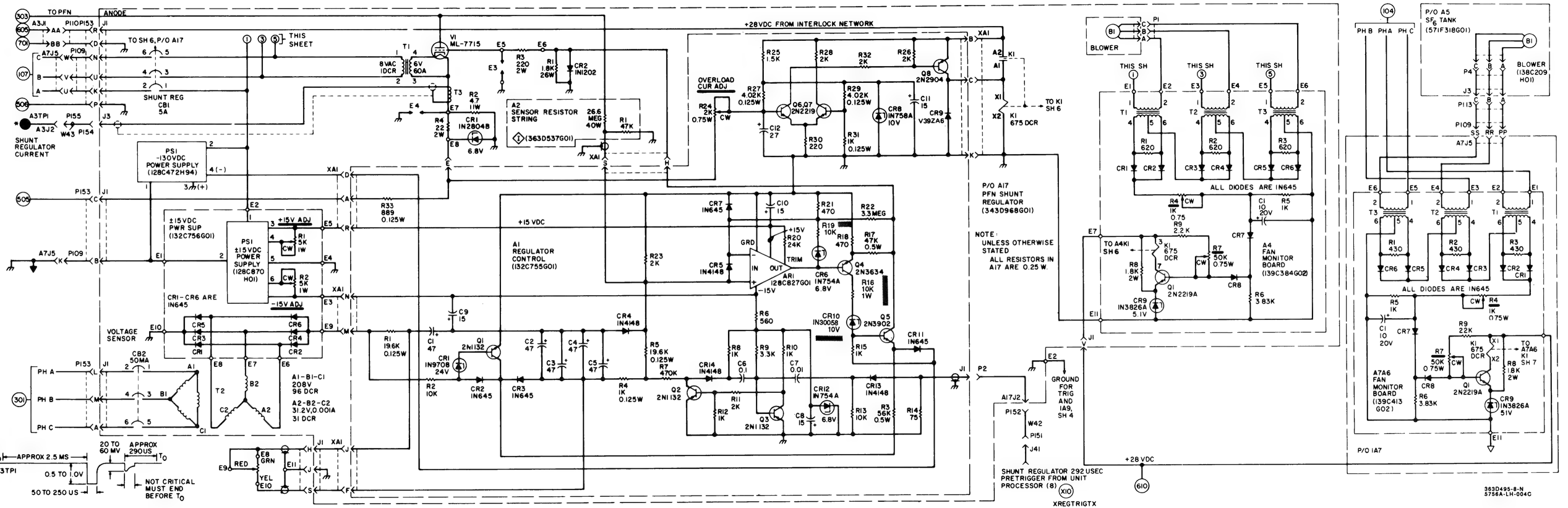


NOT TO SCALE
REFERENCE ONLY

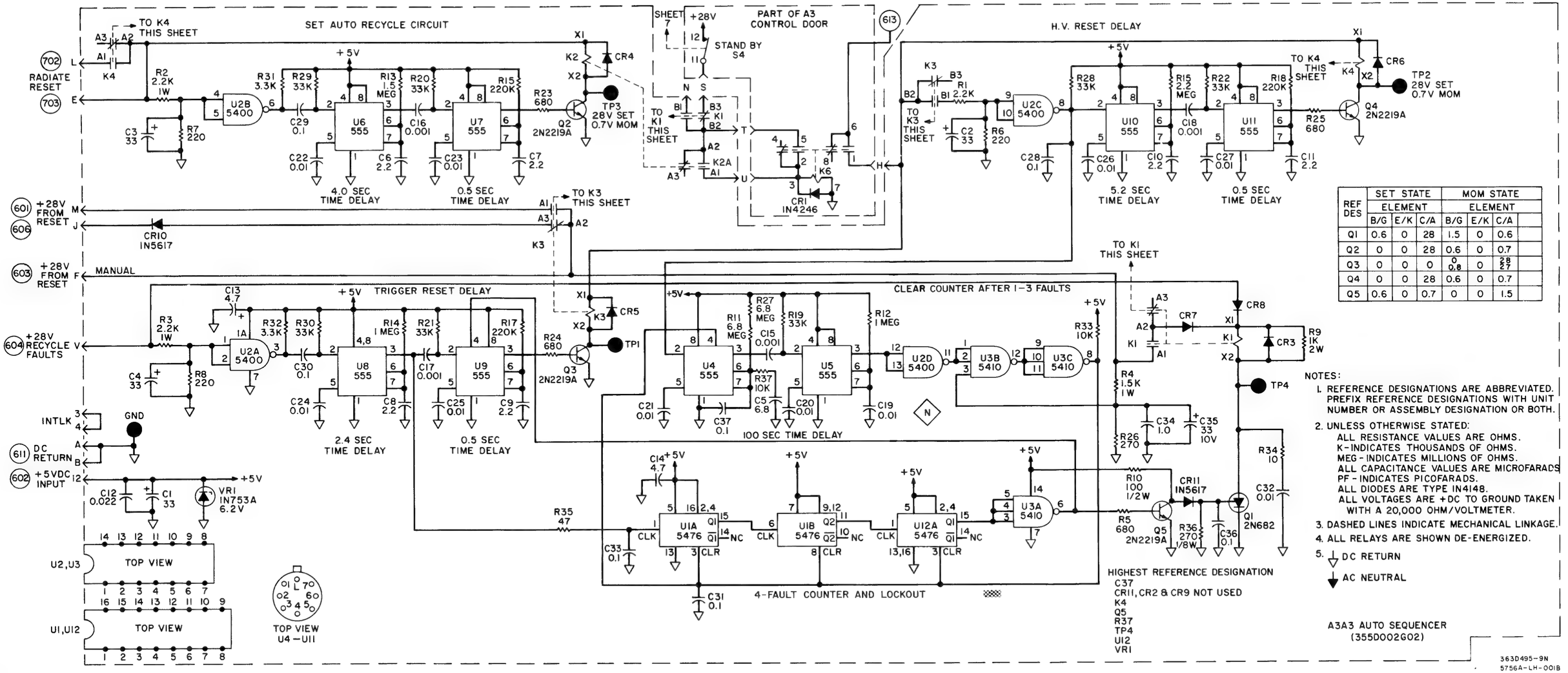
8229A-LH-020B
3630495-7N

Change 7

FO-36. (H) (T) (N) Transmitter (615J745) Schematic Diagram (Sheet 7 of 12)



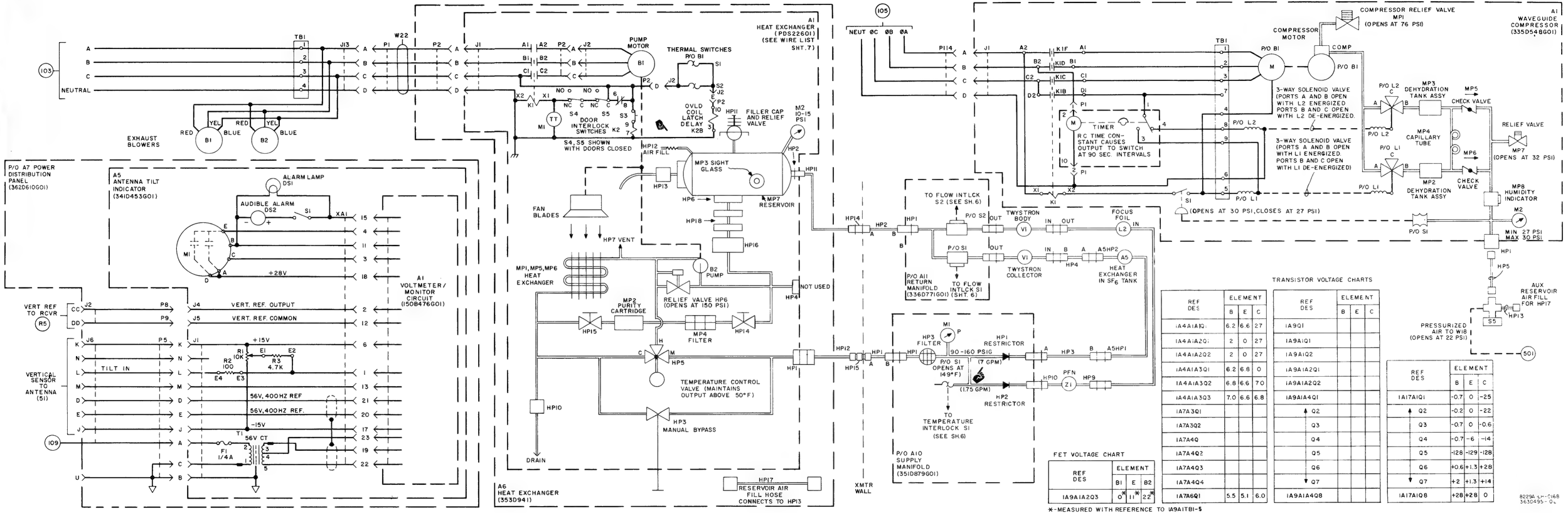
Change 11 FO-36. Ⓗ Ⓘ Ⓝ Transmitter
(615J745) Schematic Diagram
(Sheet 8 of 12)



REF DES	SET STATE			MOM STATE		
	ELEMENT			ELEMENT		
	B/G	E/K	C/A	B/G	E/K	C/A
Q1	0.6	0	28	1.5	0	0.6
Q2	0	0	28	0.6	0	0.7
Q3	0	0	0	0 / 0.8	0	28 / 27
Q4	0	0	28	0.6	0	0.7
Q5	0.6	0	0.7	0	0	1.5

NOTES:

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX REFERENCE DESIGNATIONS WITH UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
2. UNLESS OTHERWISE STATED:
   ALL RESISTANCE VALUES ARE OHMS.
   K-INDICATES THOUSANDS OF OHMS.
   MEG-INDICATES MILLIONS OF OHMS.
   ALL CAPACITANCE VALUES ARE MICROFARADS
   PF-INDICATES PICOFARADS.
   ALL DIODES ARE TYPE IN4148.
   ALL VOLTAGES ARE +DC TO GROUND TAKEN WITH A 20,000 OHM/VOLTMETER.
3. DASHED LINES INDICATE MECHANICAL LINKAGE.
4. ALL RELAYS ARE SHOWN DE-ENERGIZED.
5. ⏚ DC RETURN
   ▼ AC NEUTRAL



TRANSISTOR VOLTAGE CHARTS

REF DES	ELEMENT B	E	C
IA4A1A1Q1	6.2	6.6	27
IA4A1A2Q1	2	0	27
IA4A1A2Q2	2	0	27
IA4A1A3Q1	6.2	6.8	0
IA4A1A3Q2	6.8	6.6	7.0
IA4A1A3Q3	7.0	6.6	6.8
IA7A3Q1			
IA7A3Q2			
IA7A4Q			
IA7A4Q2			
IA7A4Q3			
IA7A4Q4			
IA7A6Q1	5.5	5.1	6.0

REF DES	ELEMENT B	E	C
IA9Q1			
IA9A1Q1			
IA9A1Q2			
IA9A1A2Q1			
IA9A1A2Q2			
IA9A1A4Q1			
↑ Q2			
Q3			
Q4			
Q5			
Q6			
↓ Q7			
IA9A1A4Q8			

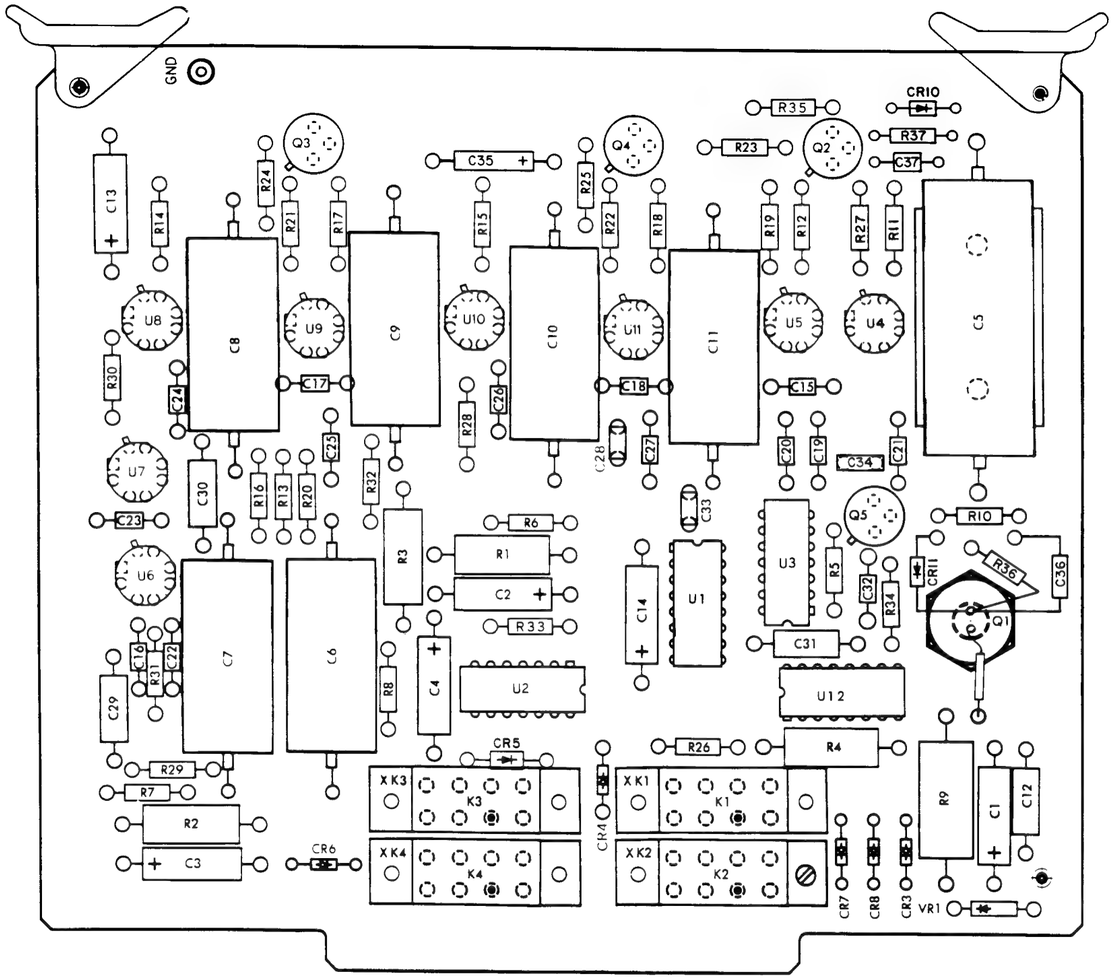
REF DES	ELEMENT B	E	C
IA17A1Q1	-0.7	0	-25
↑ Q2	-0.2	0	-22
Q3	-0.7	0	-0.6
Q4	-0.7	-6	-14
Q5	-128	-129	-128
Q6	+0.6	+1.3	+28
↓ Q7	+2	+1.3	+14
IA17A1Q8	+28	+28	0

FET VOLTAGE CHART

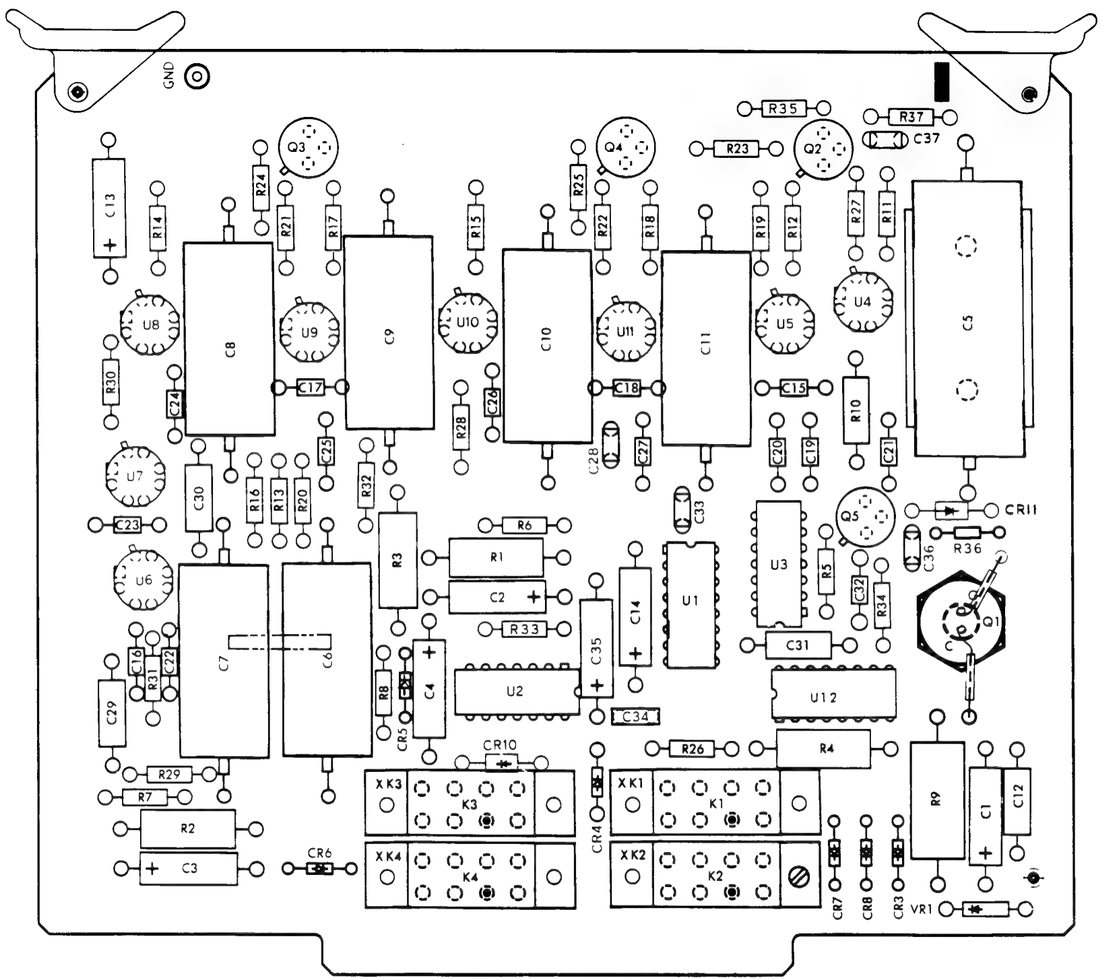
REF DES	ELEMENT B1	E	B2
IA9A1A2Q3	0*	11*	22*

*-MEASURED WITH REFERENCE TO IA9A1TB1-5

8229A LH-0168
3630495-04

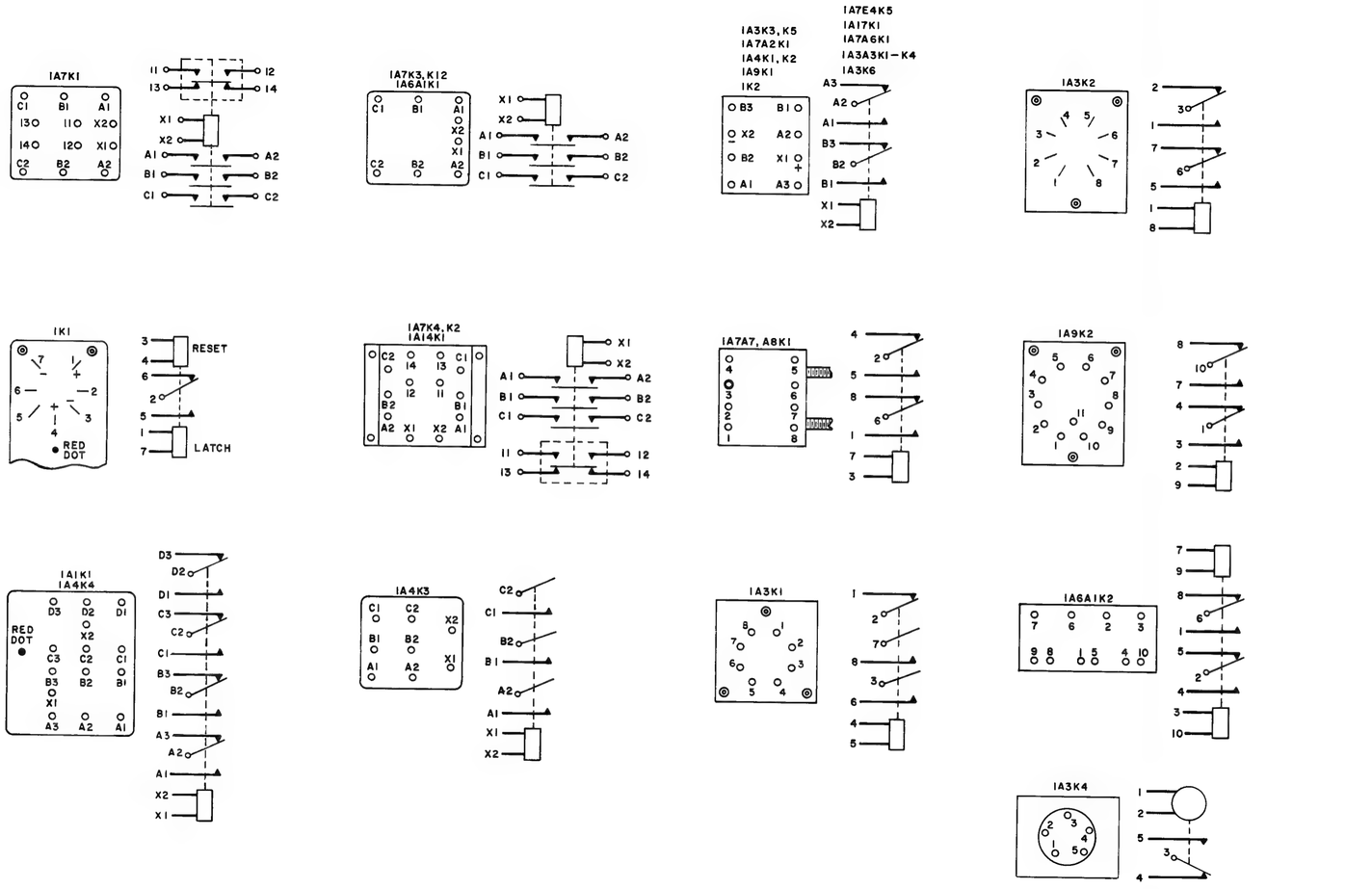


COMPONENT LAYOUT AFTER
T.C.T.O. 31P3-2TPS43-575

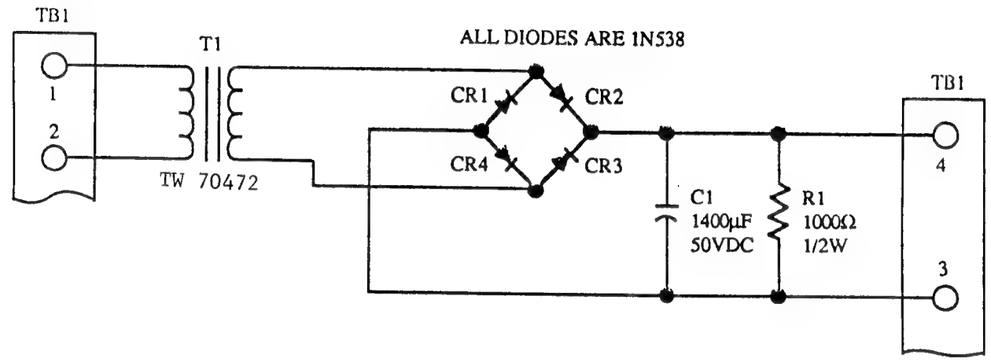


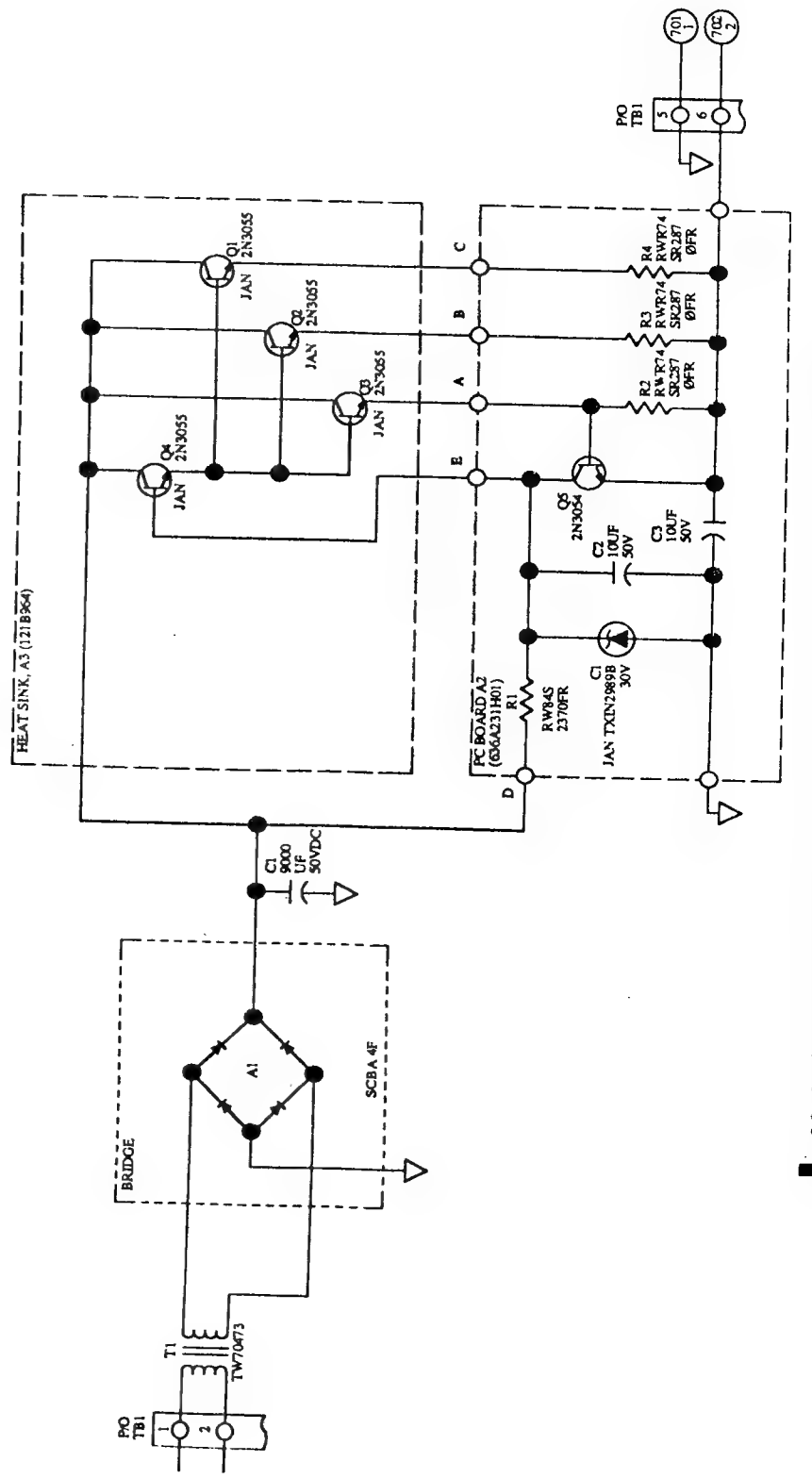
COMPONENT LAYOUT AS
MANUFACTURED BY WESTINGHOUSE

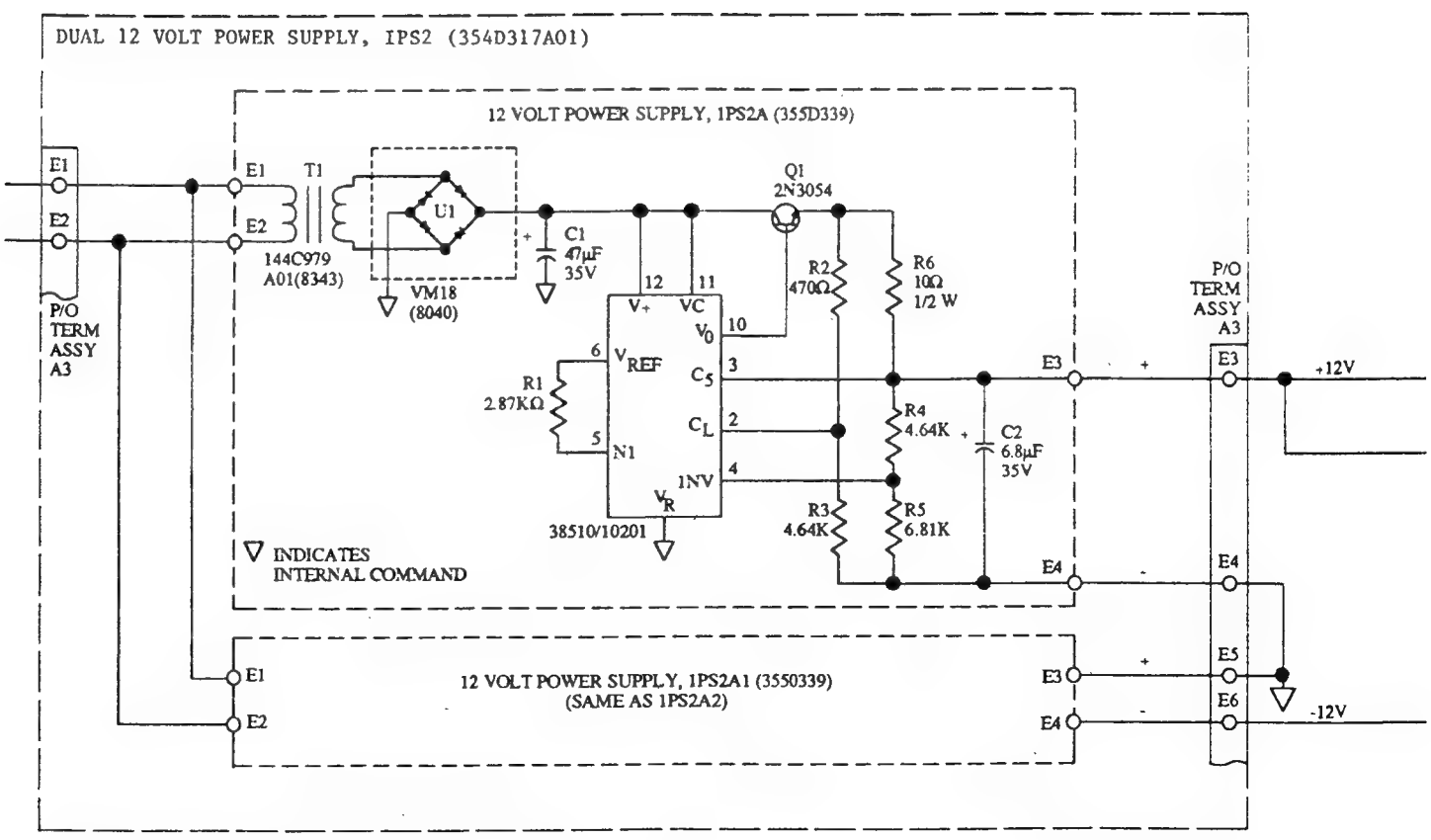
363D495-11N



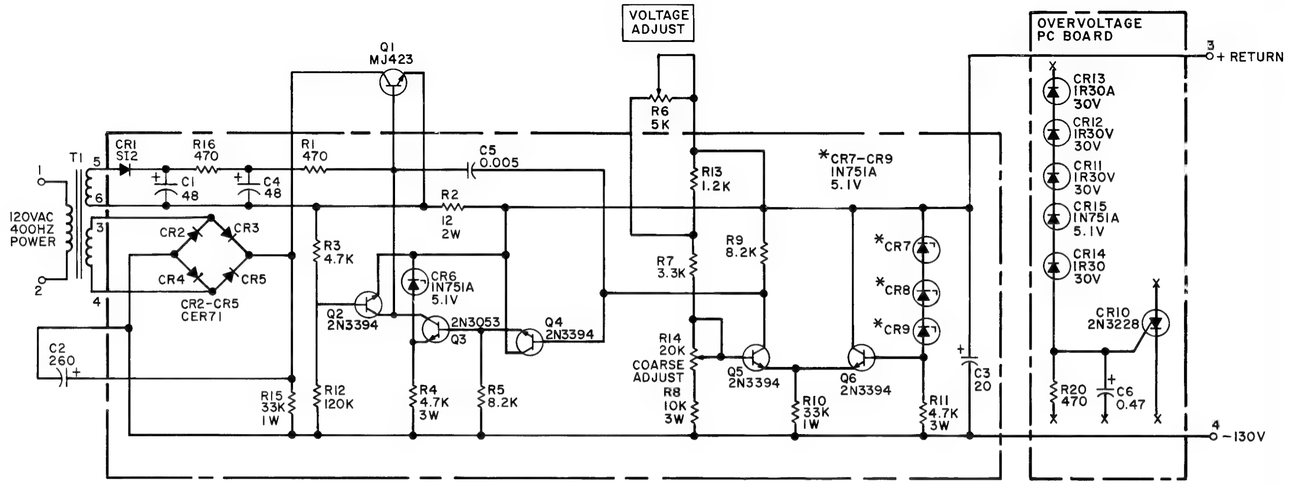
8229A-LD-104A

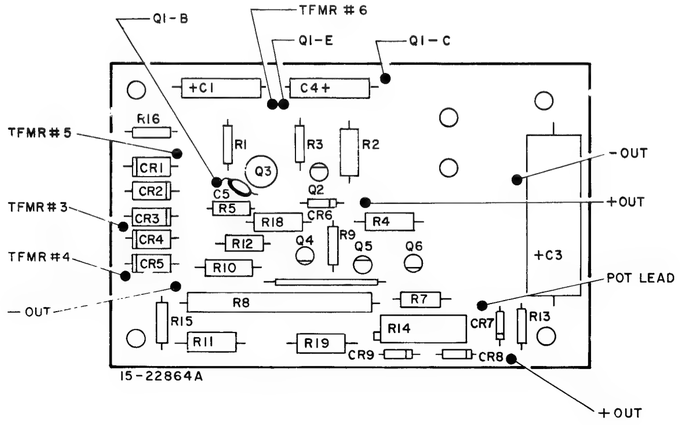

TB1
1
2
T1
TW 70472
ALL DIODES ARE 1N538
CR1
CR2
CR3
CR4
C1
1400µF
50VDC
R1
1000Ω
1/2W
TB1
4
3


J701
J702
P/O TB1
5
6
HEAT SINK, A3 (1218364)
PC BOARD A2 (8364231H01)
Q1 2N3055 JAN
Q2 2N3055 JAN
Q3 2N3055 JAN
Q4 2N3055 JAN
Q5 2N3054
R1 RW84S 2370FR
R2 RWR74 SR2S7 6FR
R3 RWR74 SR2S7 6FR
R4 RWR74 SR2S7 6FR
C1 JAN TXDN2989B 30V
C2 10UF 50V
C3 10UF 50V
C4 9000 UF 50VDC
A1 BRIDGE
SCBA 4F
T1 TW70473
P/O TB1
1
2
28 Volt Power Supply (354D318A01) Schematic Diagram



12 Volt Power Supply IPSA1 (3550339), Schematic Diagram





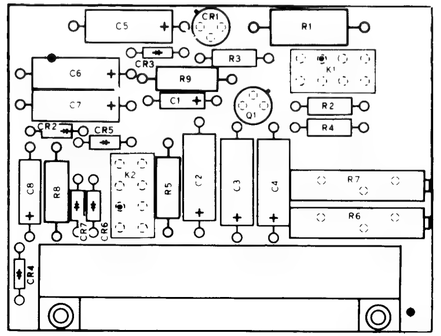
NOTES:

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX WITH THE UNIT NUMBER OR ASSEMBLY DESIGNATION OR BOTH.
2. UNLESS OTHERWISE STATED:
   ALL RESISTANCE VALUES ARE IN OHMS
   K-INDICATES THOUSANDS OF OHMS
   MEG-INDICATES MILLIONS OF OHMS
   ALL RESISTORS ARE 0.50 WATT
   ALL CAPACITANCE VALUES ARE IN MICROFARADS
   ALL VOLTAGES ARE DC TAKEN WITH A 20,000 OHM-PER-VOLT METER AND MEASURED TO GROUND.
3. CW INDICATES POSITION OF ADJUSTABLE CONTACT AT THE LIMIT OF CLOCKWISE TRAVEL WHEN VIEWED FROM THE KNOB END OR ACTUATOR END.
4. OVERVOLTAGE P.C. BOARD IS NOT USED.

TRANSISTOR VOLTAGE CHART

REF DES	ELEMENT		
	B	E	C
Q1			
Q2			
Q3			
Q4			
Q5			
Q6			

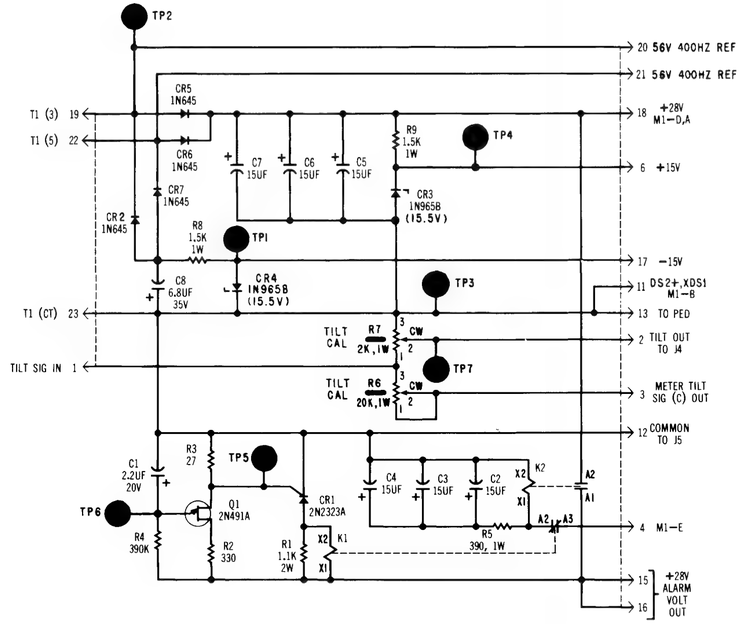
329D223-1



FET VOLTAGE CHART

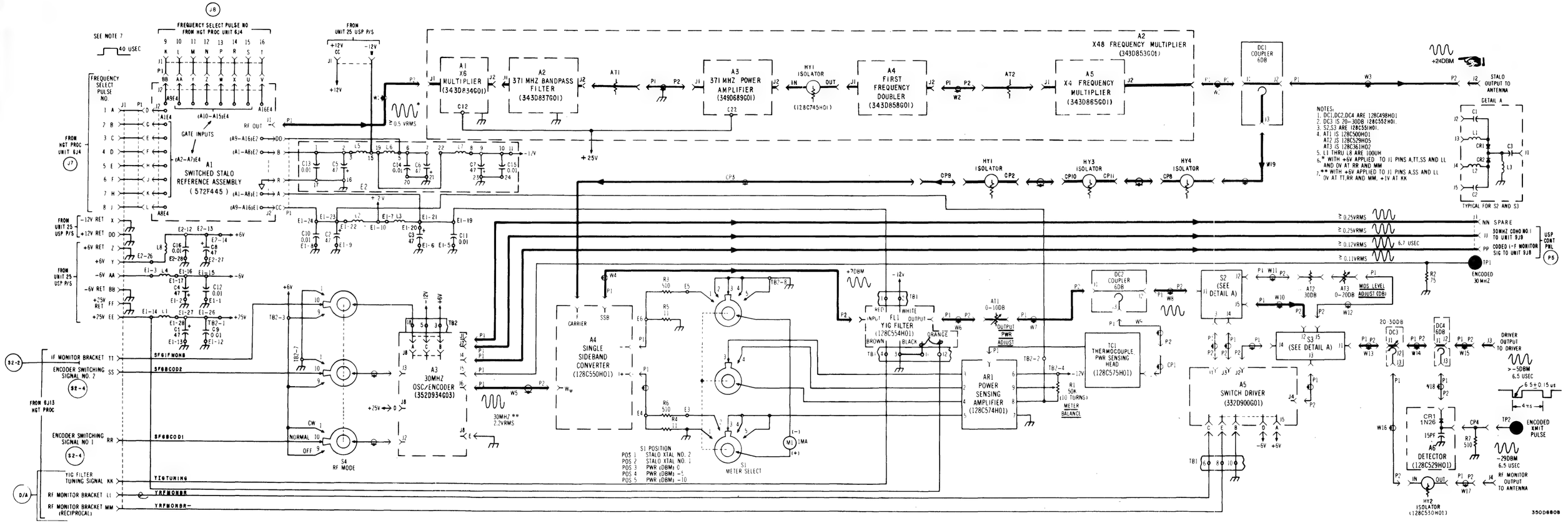
REF DES	ELEMENT		
	S	G	D
Q1	0	0	0

NOTES
1. UNLESS OTHERWISE STATED:
   ALL RESISTANCE VALUES ARE IN OHMS, 0.5W
   K-INDICATES THOUSANDS OF OHMS
   MEG-INDICATES MILLIONS OF OHMS
2. RESISTANCES OF WINDINGS LESS THAN ONE OHM ARE NOT SHOWN.
3. DOTTED LINES INDICATE MECHANICAL LINKAGE.
4. ALL RELAYS ARE SHOWN DEENERGIZED.
5. CW - INDICATES POSITION OF ADJUSTABLE CONTACT AT THE LIMIT OF CLOCKWISE TRAVEL WHEN VIEWED FROM THE KNOB END OR ACTUATOR END.

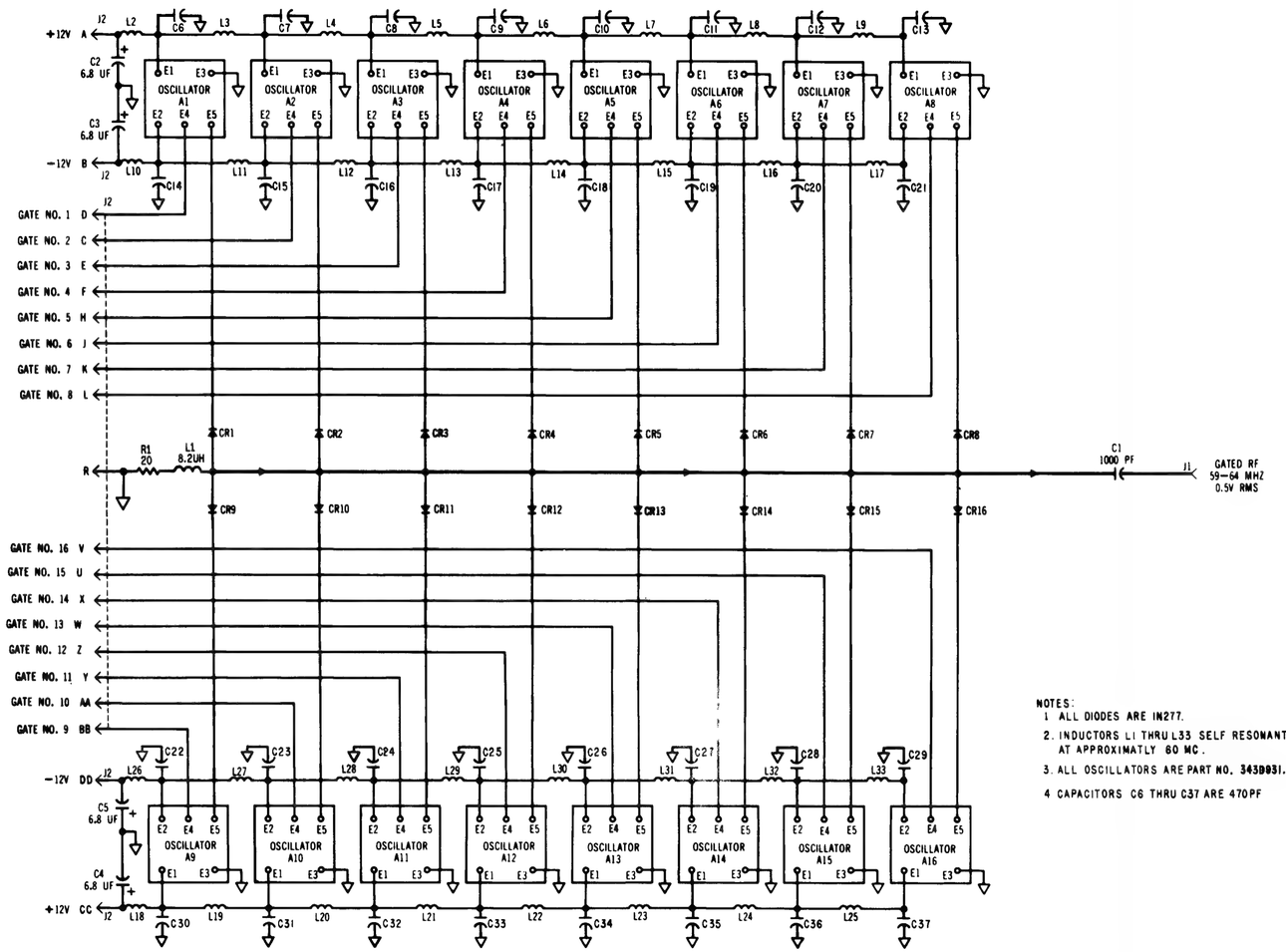


130C079D

Change 7 FO-38. Vertical Sensor (Voltmeter/Monitor) (150B476) Schematic Diagram



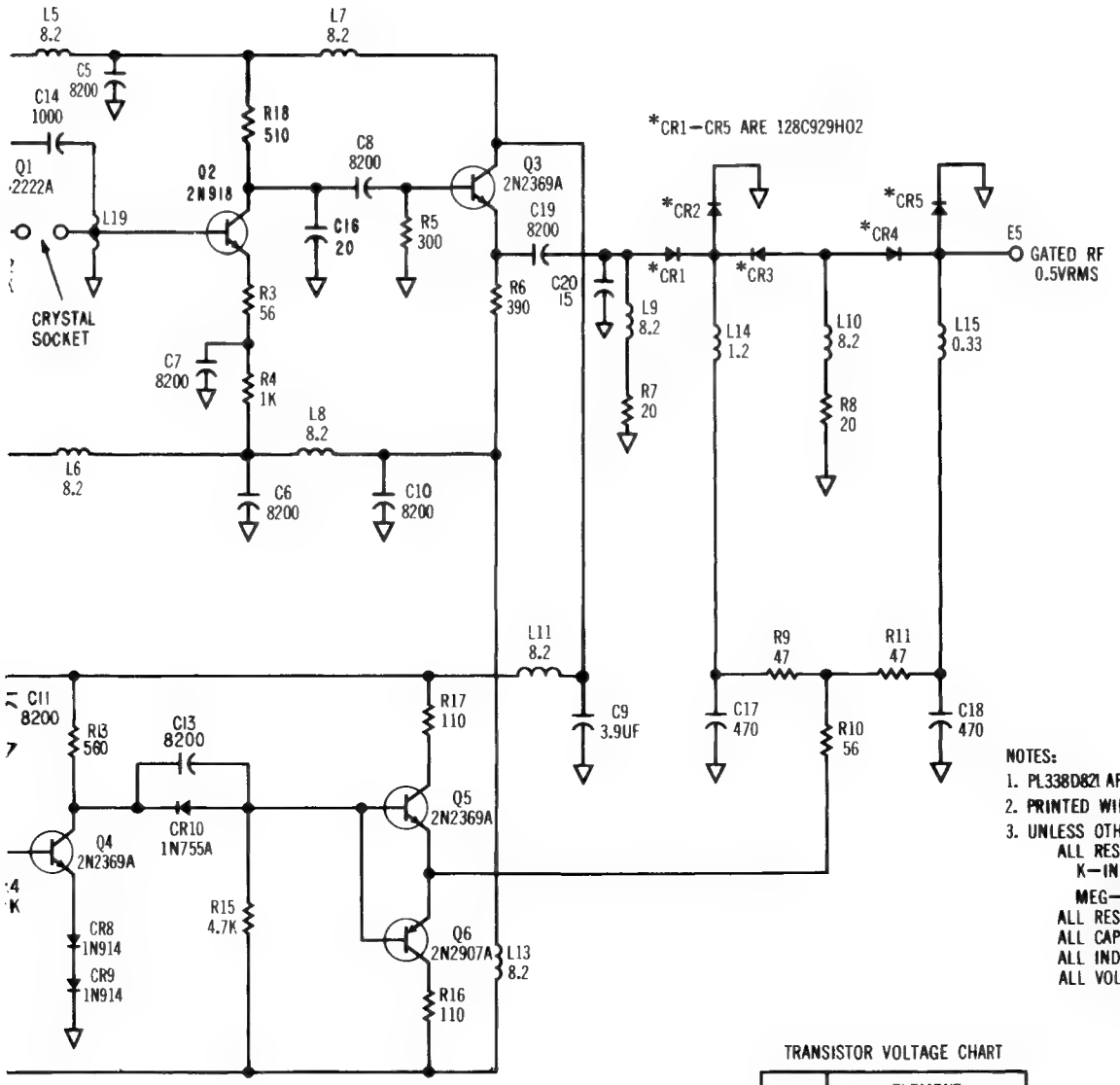
Change 9 FO-39. Signal Generator (353D985) Schematic Diagram



NOTES:
1. ALL DIODES ARE IN277.
2. INDUCTORS L1 THRU L33 SELF RESONANT AT APPROXIMATLY 60 MC.
3. ALL OSCILLATORS ARE PART NO. 343D931.
4. CAPACITORS C6 THRU C37 ARE 470PF

189C690

FO-40. Switched STALO Reference (572F445) Schematic Diagram



NOTES:
1. PL338D821 APPLIES.
2. PRINTED WIRING ASSEMBLY 338D821.
3. UNLESS OTHERWISE STATED:
   ALL RESISTANCE VALUES ARE IN OHMS
   K—INDICATES THOUSANDS OF OHMS
   MEG—INDICATES MILLIONS OF OHMS
   ALL RESISTORS ARE RCR07
   ALL CAPACITANCE VALUES ARE IN PICOFARADS
   ALL INDUCTANCE VALUES ARE IN MICROHENRIES
   ALL VOLTAGES ARE DC

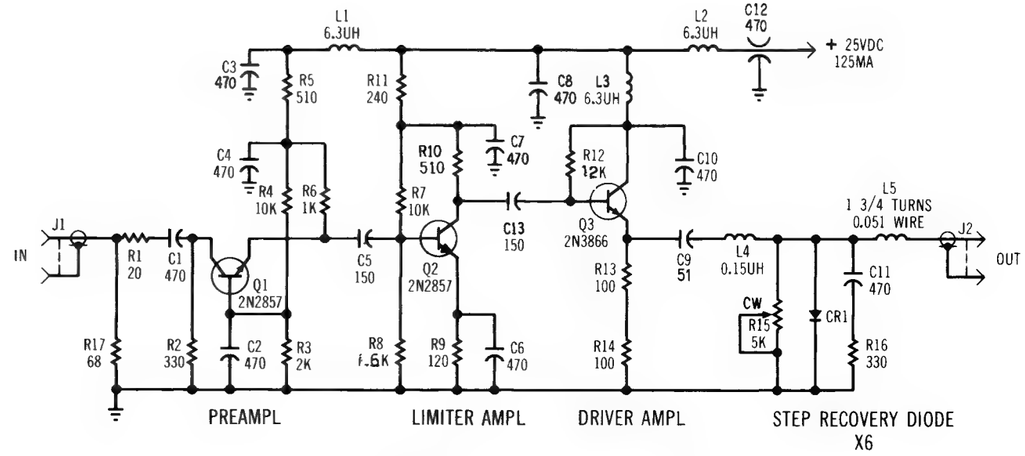
TRANSISTOR VOLTAGE CHART

REF DES	ELEMENT		
	E	B	C
Q1	−0.7	0	+7.8
Q2	−0.7	0	+12
Q3	−0.7	0	+12
Q4	+0.14	+0.2	+0.3
Q5	−6.5	−7.2	+12
Q6	−6.5	−7.2	−7.2

RF SWITCH IS ON

129C904E

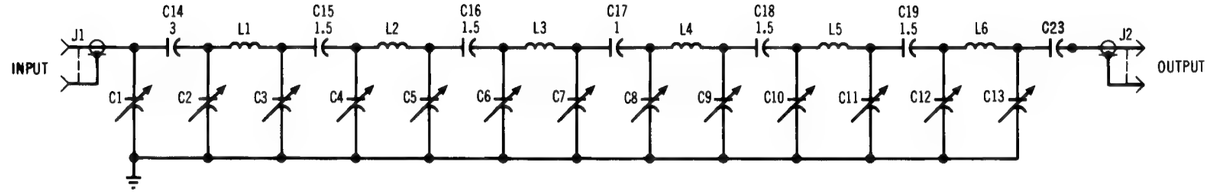
Change 7 FO-41. 60 MHz Oscillator and Oscillator Gate (343D931) Schematic Diagram



NOTE:
1. ALL CAPACITANCE VALUES IN PICOFARADS.

130C295C

Change 6 FO-42. X6 Multiplier (343D834) Schematic Diagram



PARTS:

C1 THRU C13 1—10PF

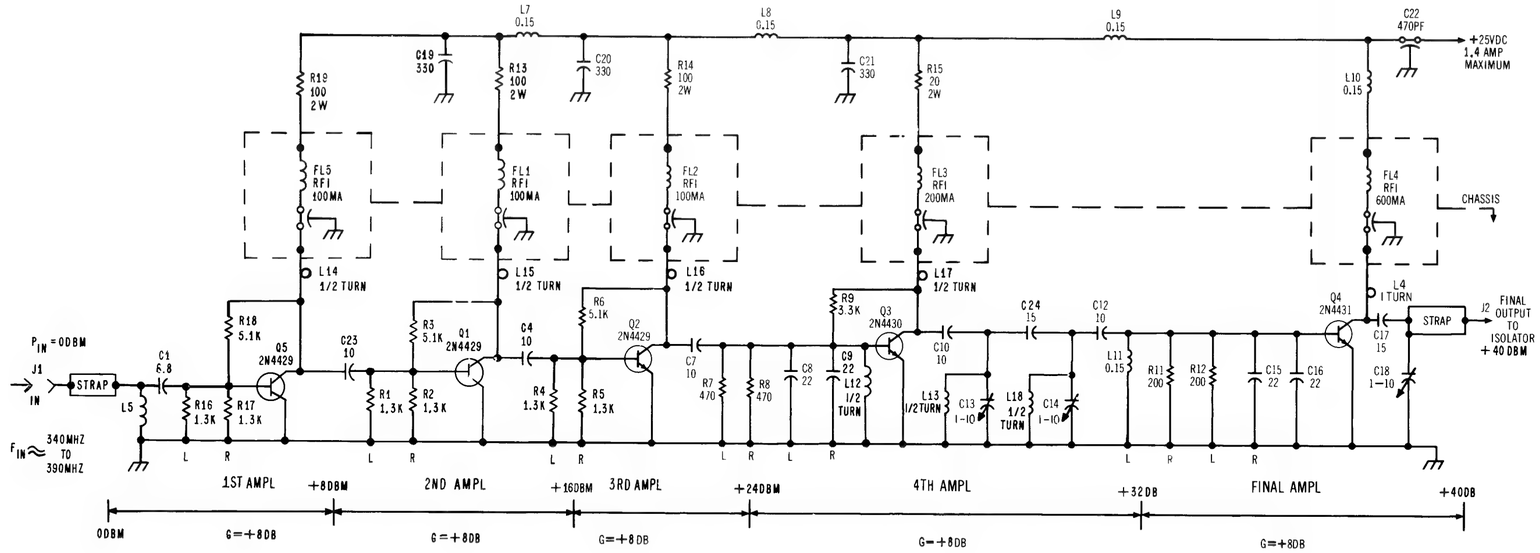
L1 THRU L6 3 TURNS NO. 16, 3/16 INCH I.D.

NOTE:

1. ALL CAPACITANCE VALUES IN PICOFARADS.

130C291

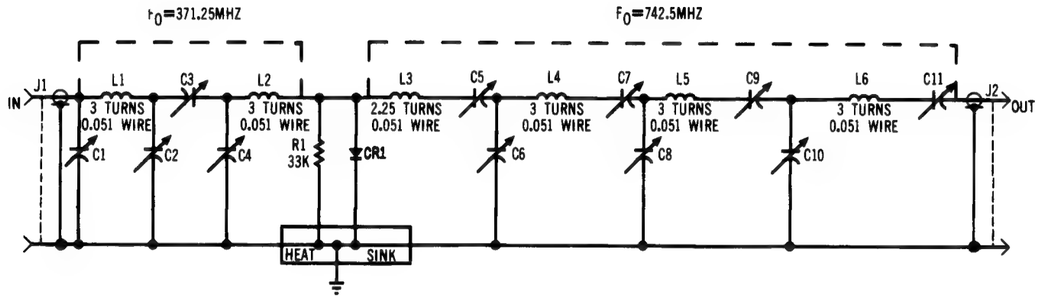
FO-43. 371MHz Band Pass Filter (343D837) Schematic Diagram



ALL CIRCUITRY BELOW RFI FILTERS IS MOUNTED ON A SYMMETRICAL GND PLANE P.C. BOARD.
R INDICATES RIGHT SIDE OF BOARD.
L INDICATES LEFT SIDE OF BOARC.

NOTES:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE VALUES ARE IN OHMS
K—INDICATES THOUSANDS OF OHMS
ALL RESISTORS ARE 1/8 WATT
ALL CAPACITANCE VALUES ARE IN PICOFARADS
UF—INDICATES MICROFARADS
ALL INDUCTANCE VALUES ARE IN MILLIHENRIES

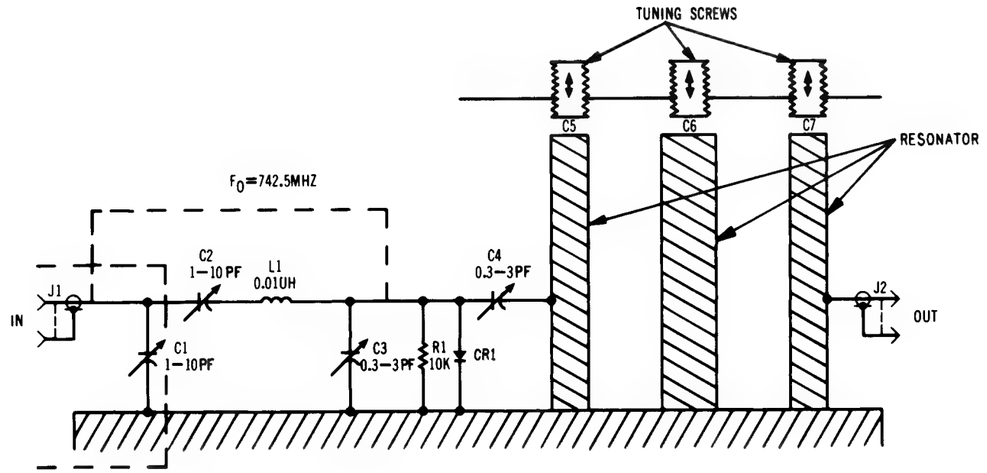
129C894—A



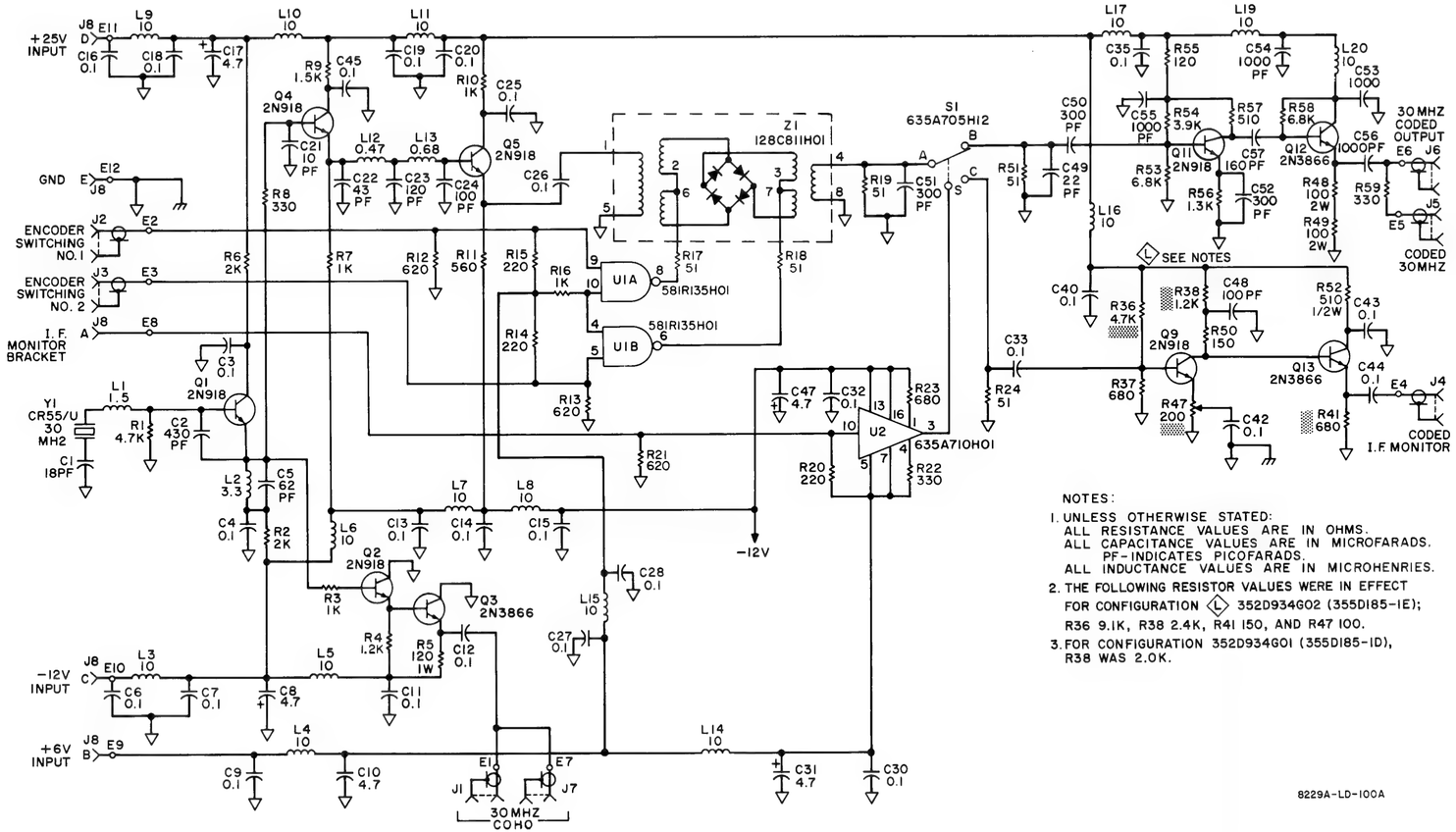
NOTES:
1. C1 THRU C4, C6, C8, C10 ARE 1-10 PF.
2. C5, C7, C9, C11 ARE 0.3-3 PF.

130C293

FO-45. First Frequency Doubler (343D858) Schematic Diagram



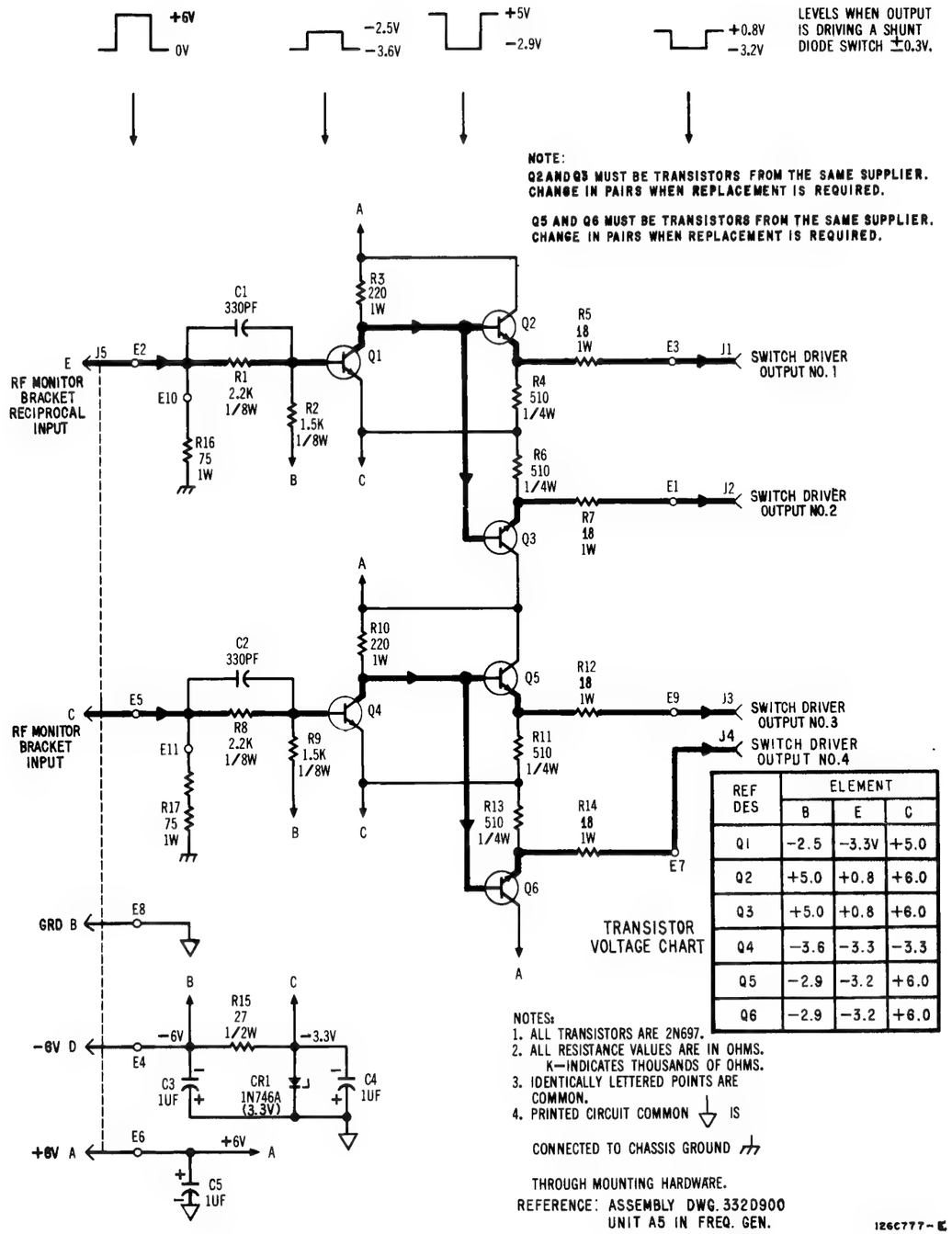
FO-46. X4 Frequency Multiplier (343D865) Schematic Diagram



NOTES:

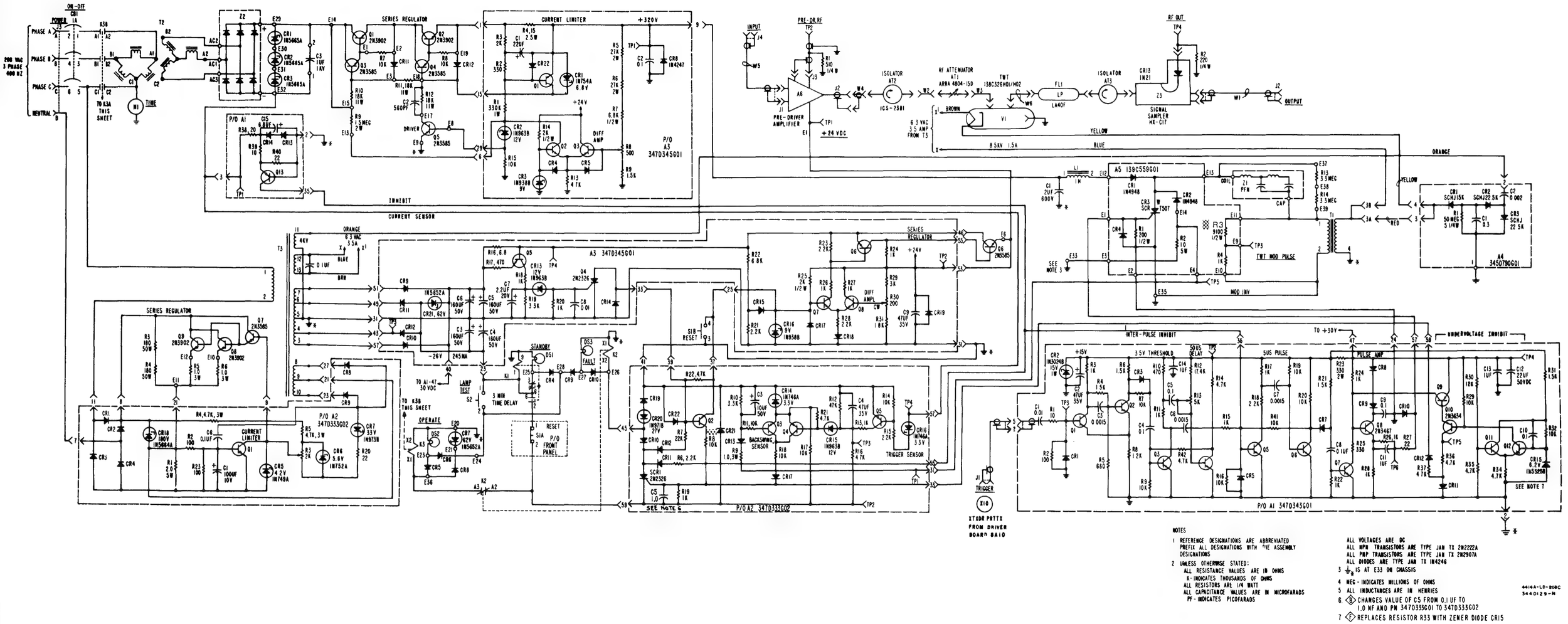
1. UNLESS OTHERWISE STATED:
   ALL RESISTANCE VALUES ARE IN OHMS.
   ALL CAPACITANCE VALUES ARE IN MICROFARADS.
   PF-INDICATES PICOFARADS.
   ALL INDUCTANCE VALUES ARE IN MICROHENRIES.
2. THE FOLLOWING RESISTOR VALUES WERE IN EFFECT FOR CONFIGURATION ◇L◇ 352D934G02 (355D185-1E); R36 9.1K, R38 2.4K, R41 150, AND R47 100.
3. FOR CONFIGURATION 352D934G01 (355D185-1D), R38 WAS 2.0K.

FO-47. 30 MHz Oscillator/Encoder (◇O◇ 352D934G03) Schematic Diagram



Change 6

FO-48. Microwave Switch Driver (332D900) Schematic Diagram

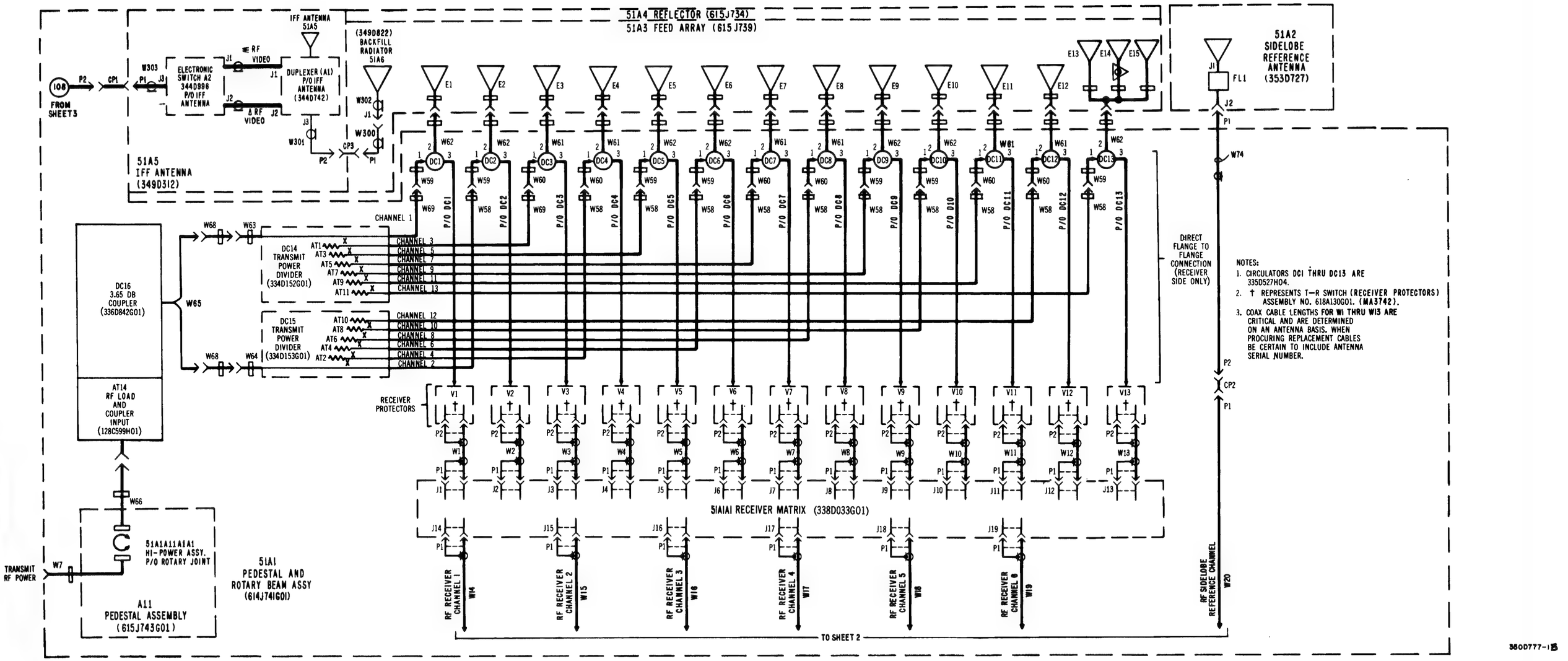


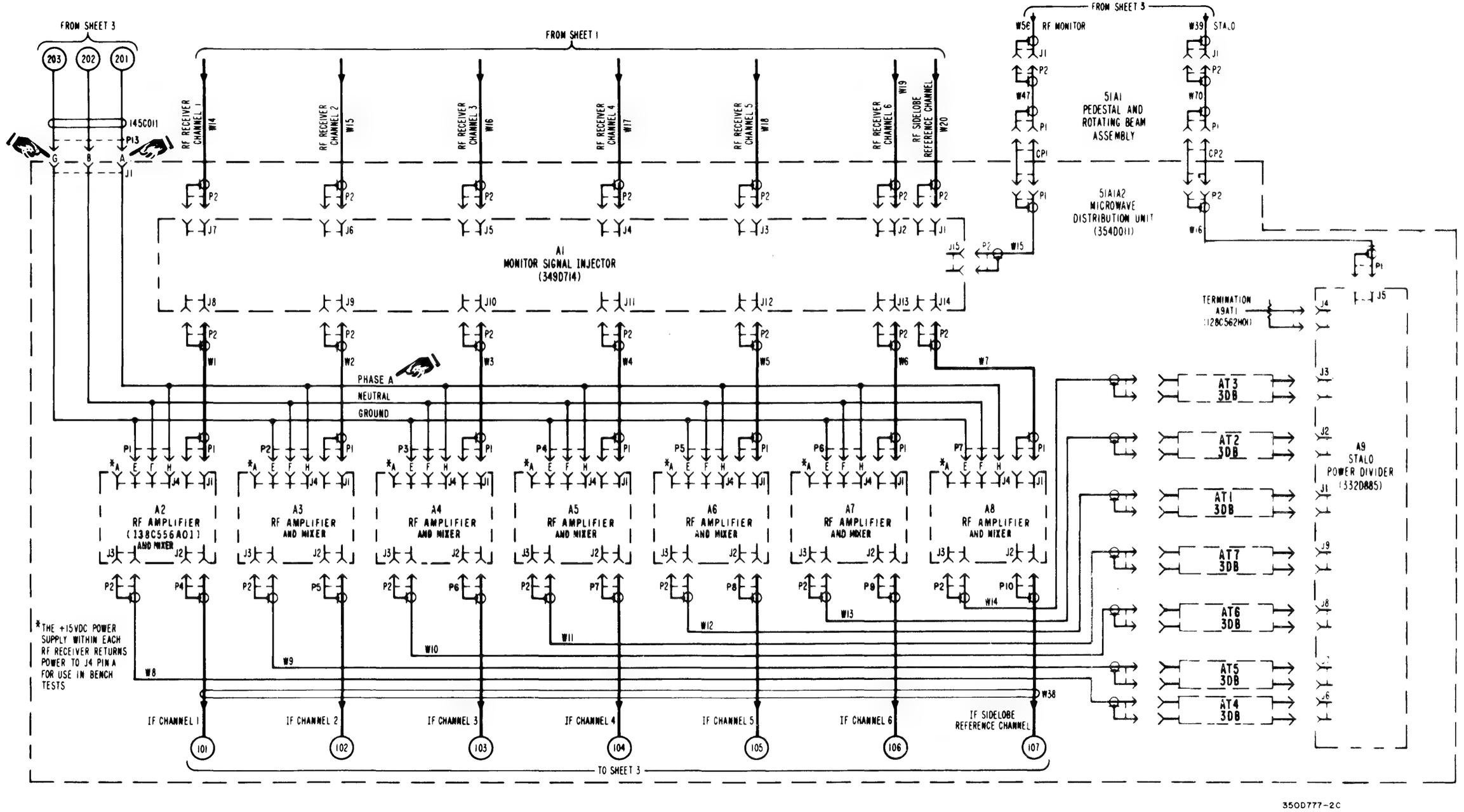
NOTES

1. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX ALL DESIGNATIONS WITH THE ASSEMBLY DESIGNATIONS
2. UNLESS OTHERWISE STATED:
   - ALL RESISTANCE VALUES ARE IN OHMS
   - K-INDICATES THOUSANDS OF OHMS
   - ALL RESISTORS ARE 1/4 WATT
   - ALL CAPACITANCE VALUES ARE IN MICROFARADS
   - PF-INDICATES PICOFARADS

   ALL VOLTAGES ARE DC
   ALL NPN TRANSISTORS ARE TYPE JAN TX 2N2222A
   ALL PNP TRANSISTORS ARE TYPE JAN TX 2N2907A
   ALL DIODES ARE TYPE JAN TX IN4246
3. ⏚ IS AT E33 ON CHASSIS
4. MEG-INDICATES MILLIONS OF OHMS
5. ALL INDUCTANCES ARE IN HENRIES
6. ◇ CHANGES VALUE OF C5 FROM 0.1 UF TO 1.0 MF AND PN 3470333G01 TO 3470333G02
7. ◇ REPLACES RESISTOR R33 WITH ZENER DIODE CR15

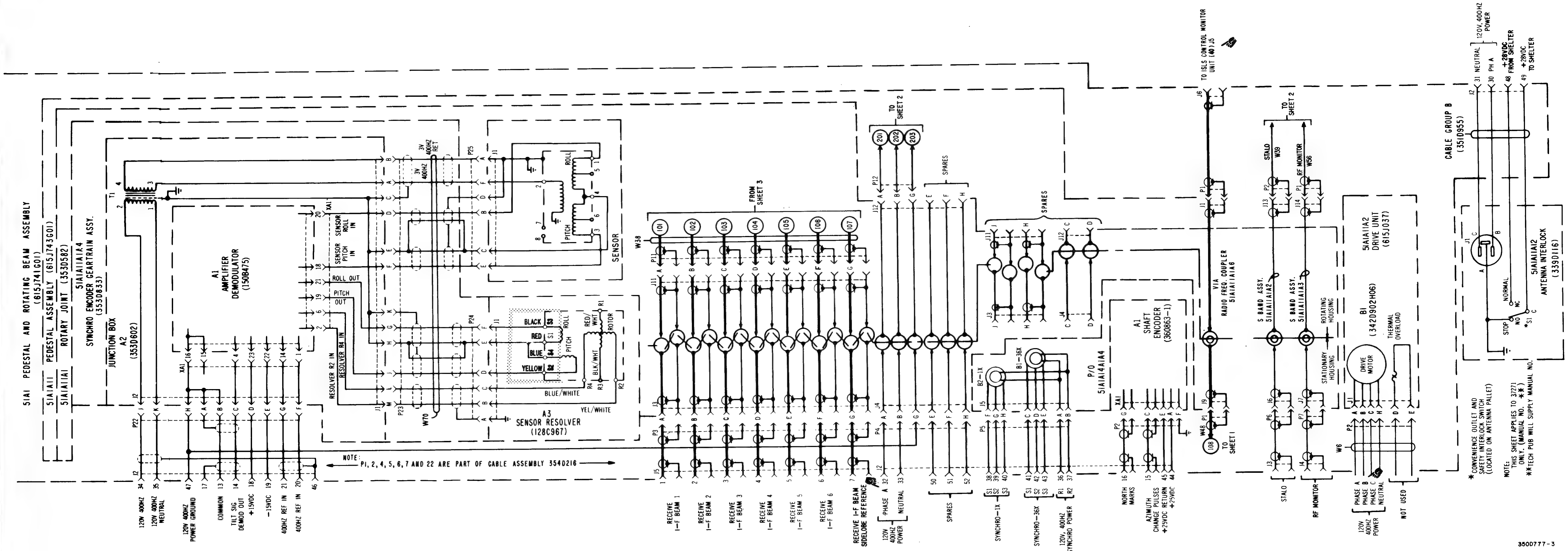
4414A-LD-208C
3440129-N

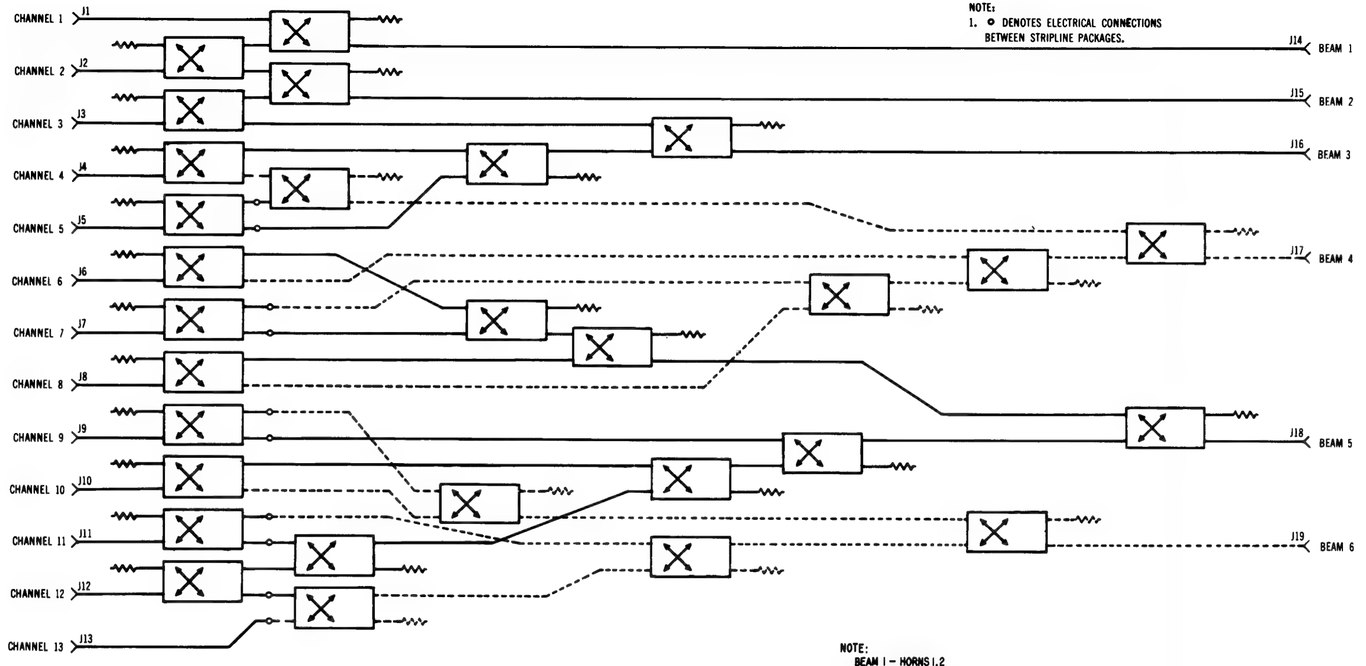

51A4 REFLECTOR (615J734)
51A3 FEED ARRAY (615J739)
51A2 SIDELOBE REFERENCE ANTENNA (353D727)
IFF ANTENNA 51A5
(349D822) BACKFILL RADIATOR 51A6
ELECTRONIC SWITCH A2 344D996 P/O IFF ANTENNA
DUPLEXER (A1) P/O IFF ANTENNA (344D742)
RF VIDEO
Δ RF VIDEO
FROM SHEET3
51A5 IFF ANTENNA (349D312)
DC16 3.65 DB COUPLER (336D842G01)
AT14 RF LOAD AND COUPLER INPUT (128C599H01)
DC14 TRANSMIT POWER DIVIDER (334D152G01)
DC15 TRANSMIT POWER DIVIDER (334D153G01)
CHANNEL 1
CHANNEL 3
CHANNEL 5
CHANNEL 7
CHANNEL 9
CHANNEL 11
CHANNEL 13
CHANNEL 12
CHANNEL 10
CHANNEL 8
CHANNEL 6
CHANNEL 4
CHANNEL 2
RECEIVER PROTECTORS
51A1A1 RECEIVER MATRIX (338D033G01)
DIRECT FLANGE TO FLANGE CONNECTION (RECEIVER SIDE ONLY)
TRANSMIT RF POWER
51A1A11A1A1 HI-POWER ASSY. P/O ROTARY JOINT
51A1 PEDESTAL AND ROTARY BEAM ASSY (614J741G01)
A11 PEDESTAL ASSEMBLY (615J743G01)
RF RECEIVER CHANNEL 1
RF RECEIVER CHANNEL 2
RF RECEIVER CHANNEL 3
RF RECEIVER CHANNEL 4
RF RECEIVER CHANNEL 5
RF RECEIVER CHANNEL 6
RF SIDELOBE REFERENCE CHANNEL
TO SHEET 2
NOTES:
1. CIRCULATORS DC1 THRU DC13 ARE 335D527H04.
2. † REPRESENTS T-R SWITCH (RECEIVER PROTECTORS) ASSEMBLY NO. 618A130G01. (MA3742).
3. COAX CABLE LENGTHS FOR W1 THRU W13 ARE CRITICAL AND ARE DETERMINED ON AN ANTENNA BASIS. WHEN PROCURING REPLACEMENT CABLES BE CERTAIN TO INCLUDE ANTENNA SERIAL NUMBER.
360D777-1B



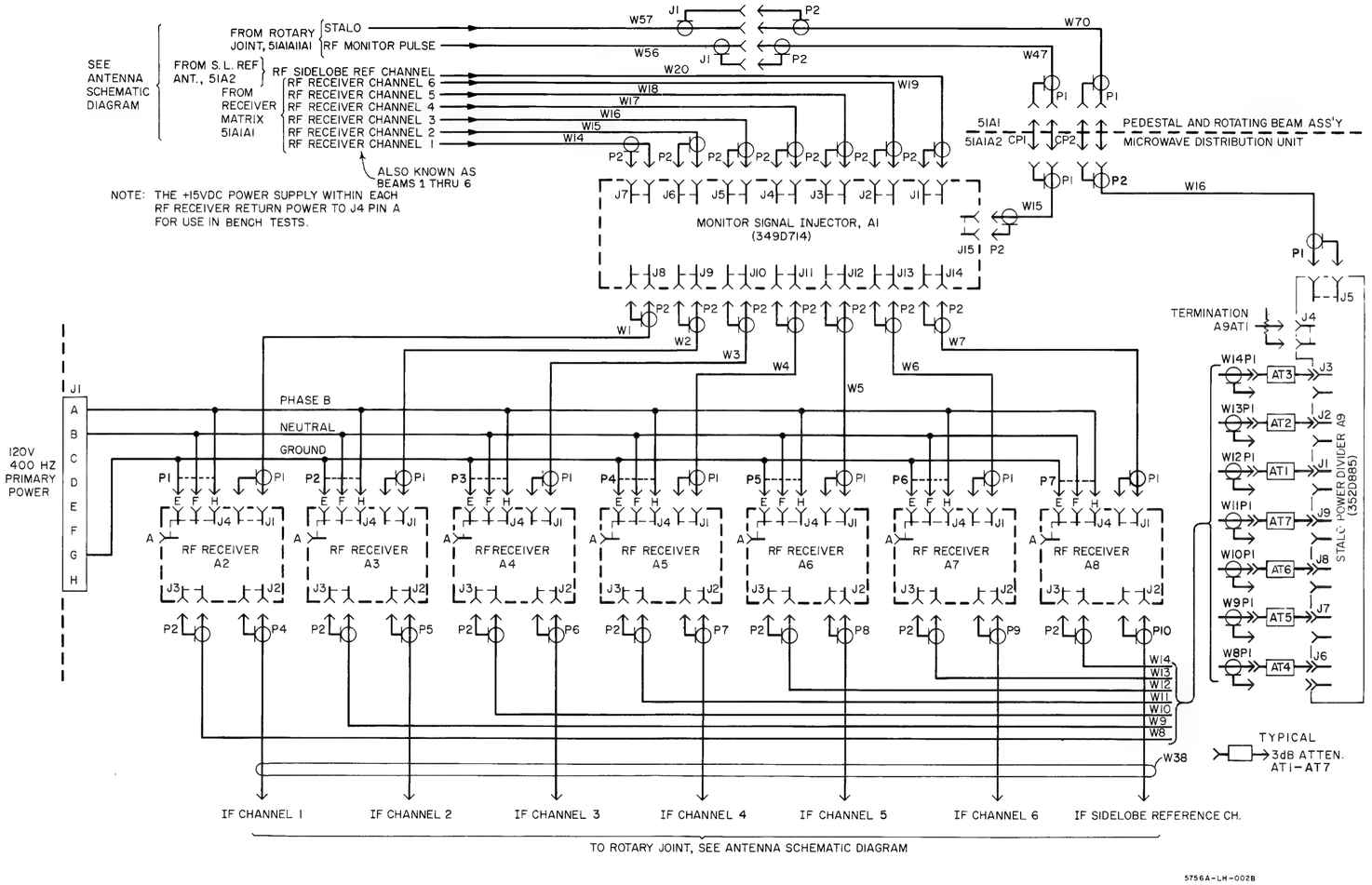
350D777-2C

Change 9 *FO-50. Antenna Assembly (615J733) Schematic Diagram (Sheet 2 of 3)*

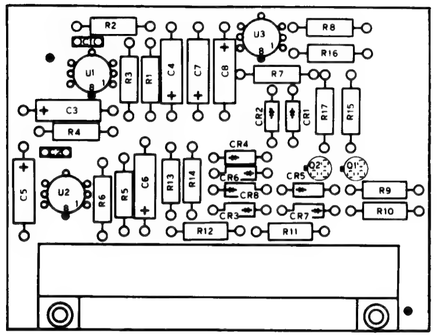

5IAI PEDESTAL AND ROTATING BEAM ASSEMBLY (615J741G01)
5IAIA11 PEDESTAL ASSEMBLY (615J743G01)
5IAIA11A1 ROTARY JOINT (3530582)
5IAIA11A1A4 SYNCHRO ENCODER GEARTRAIN ASSY. (3530833)
JUNCTION BOX A2 (3530802)
A1 AMPLIFIER DEMODULATOR (1508475)
A3 SENSOR RESOLVER (128C967)
SENSOR
ROLL
PITCH
BLACK
RED
BLUE
YELLOW
BLUE/WHITE
YEL/WHITE
RED/WHT
BLK/WHT
ROTOR
ROLL OUT
PITCH OUT
SENSOR ROLL IN
SENSOR PITCH IN
RESOLVER R2 IN
RESOLVER R4 IN
3V 400HZ
3V 400HZ RET
W70
W38
FROM SHEET 3
TO SHEET 2
SPARES
NOTE: P1, 2, 4, 5, 6, 7 AND 22 ARE PART OF CABLE ASSEMBLY 3540216
120V 400HZ
120V 400HZ NEUTRAL
120V 400HZ POWER GROUND
COMMON
TILT SIG DEMOD OUT
+15VDC
-15VDC
400HZ REF IN
400HZ REF IN
RECEIVE I-F BEAM 1
RECEIVE I-F BEAM 2
RECEIVE I-F BEAM 3
RECEIVE I-F BEAM 4
RECEIVE I-F BEAM 5
RECEIVE I-F BEAM 6
RECEIVE I-F BEAM SIDELOBE REFERENCE
120V 400HZ POWER
PHASE A
NEUTRAL
SPARES
SYNCHRO-1X
SYNCHRO-36X
120V, 400HZ SYNCHRO POWER
P/O 5IAIA14A1A4
A1 SHAFT ENCODER (360863-1)
NORTH MARKS
AZIMUTH CHANGE PULSES
+2.5VDC RETURN
+2.5VDC
TO ISLS CONTROL MONITOR UNIT (4071J5
VIA RADIO FREQ. COUPLER 5IAIA11A16
TO SHEET 1
S BAND ASSY. 5IAIA11A1A2
S BAND ASSY. 5IAIA11A1A3
STALO
RF MONITOR
ROTATING HOUSING
STATIONARY HOUSING
B1 (3420902H06)
DRIVE MOTOR
THERMAL OVERLOAD
5IAIA11A2 DRIVE UNIT (615J037)
PHASE A
PHASE B
PHASE C
NEUTRAL
NOT USED
CABLE GROUP B (3510955)
31 NEUTRAL
30 PH A
120V 400HZ POWER
48 +28VDC FROM SHELTER
49 +28VDC TO SHELTER
NORMAL
STOP
*S1
5IAIA11A2 ANTENNA INTERLOCK (3390116)
*CONVENIENCE OUTLET AND SAFETY INTERLOCK SWITCH (LOCATED ON ANTENNA PALLET)
NOTE: THIS SHEET APPLIES TO 3727J ONLY. (MANUAL NO. **)
**TECH PUB WILL SUPPLY MANUAL NO.
350D777-3



FO-51. Receiver Matrix (338D033) Schematic Diagram



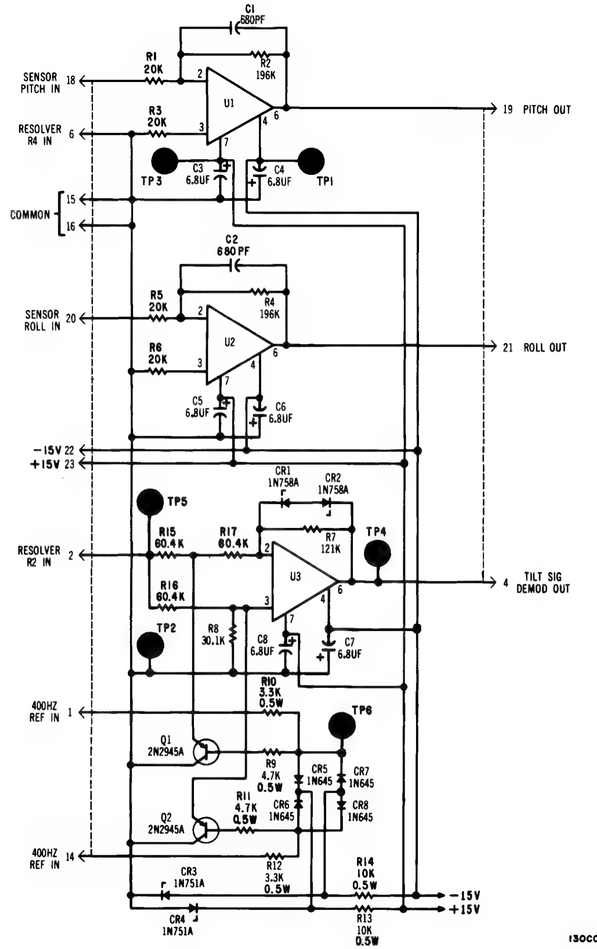
Change 7 FO-52. Microwave Distribution Unit (354D011G01) Schematic Diagram



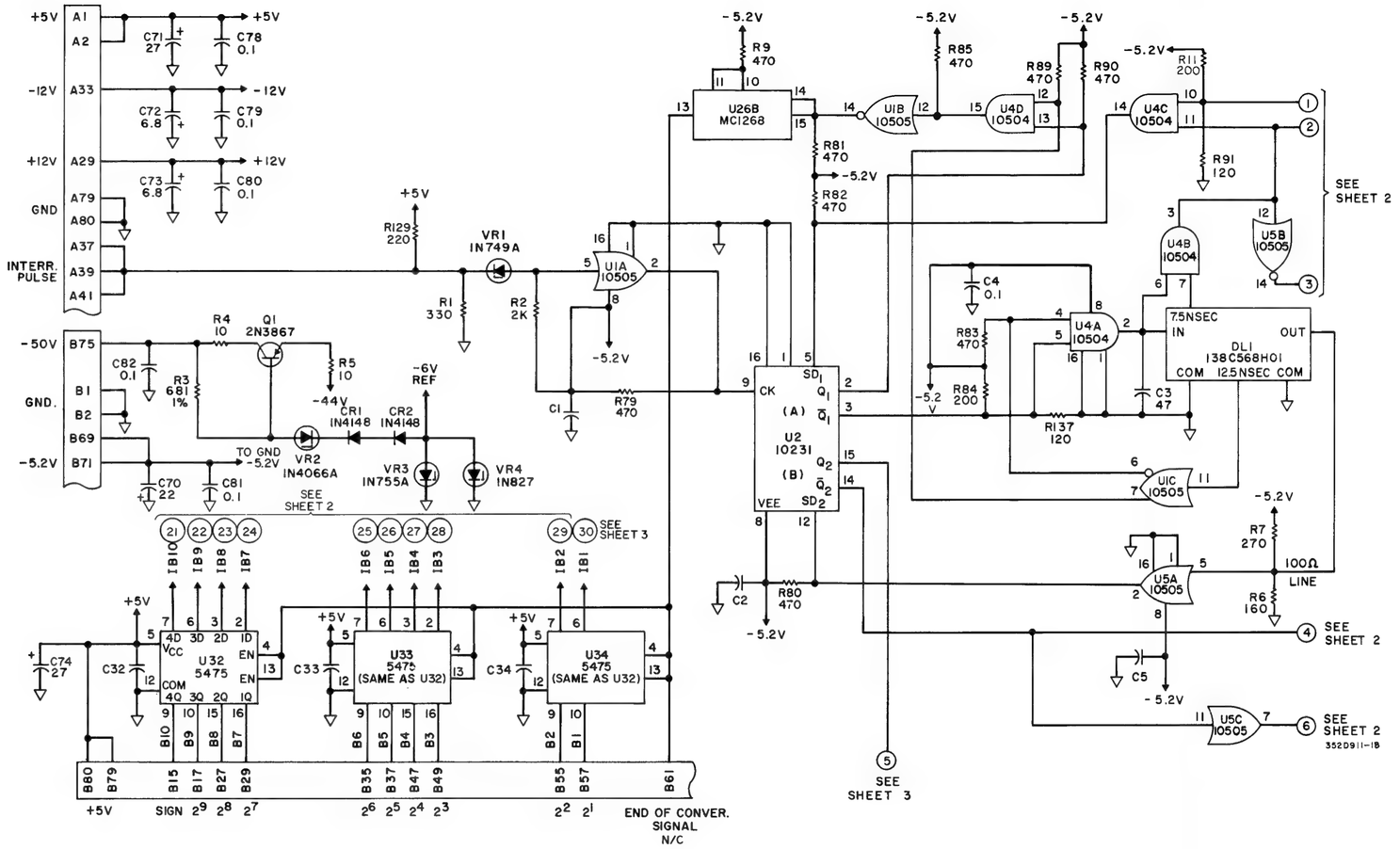
TRANSISTOR VOLTAGE CHART

REF DES	ELEMENT		
	B	E	C
Q1	2.3	0	0
Q2	2.3	0	0

NOTES
1. UNLESS OTHERWISE STATED:
   ALL RESISTANCE VALUES ARE IN OHMS, 0.25W
   K-INDICATES THOUSANDS OF OHMS
   MEG-INDICATES MILLIONS OF OHMS
2. U1,U2 AND U3 ARE 128C952H01



FO-53. Amplifier-Demodulator (150B425) Schematic Diagram

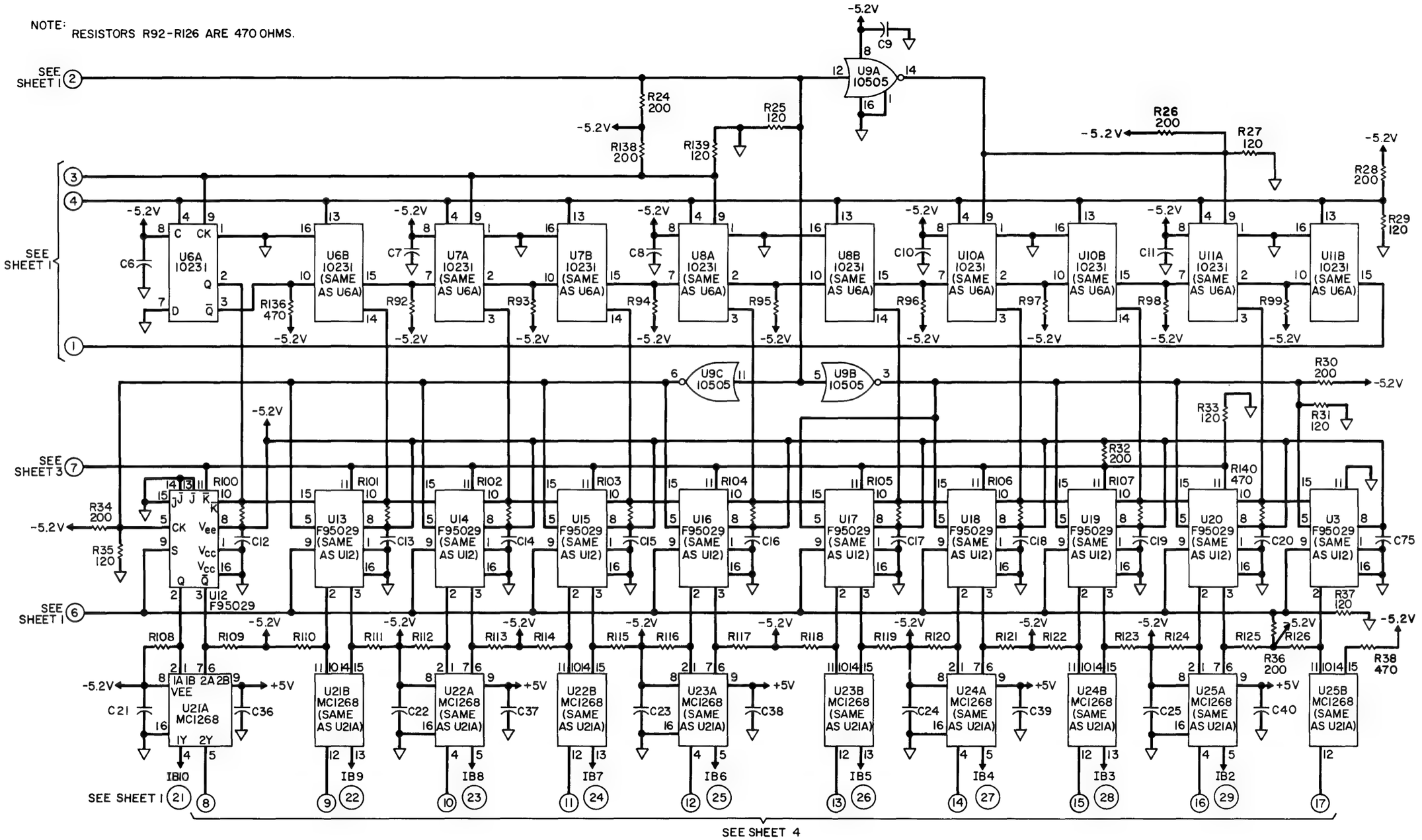


SEE NOTES ON SHEET 4

352D911-1B

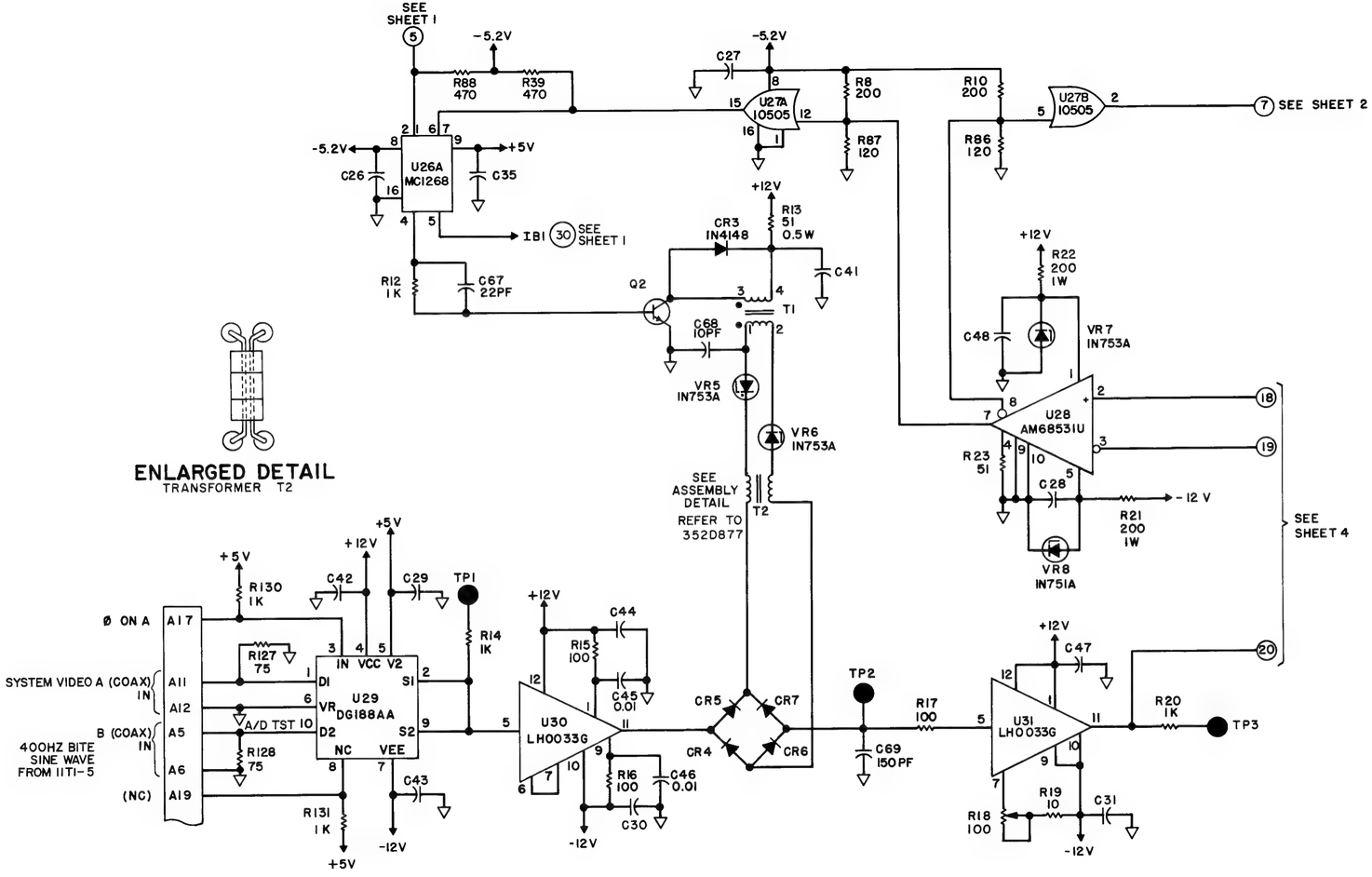
Change 7 FO-54. Alternate A/D Converter Printed Circuit (352D877G01) Schematic Diagram (Sheet 1 of 4)

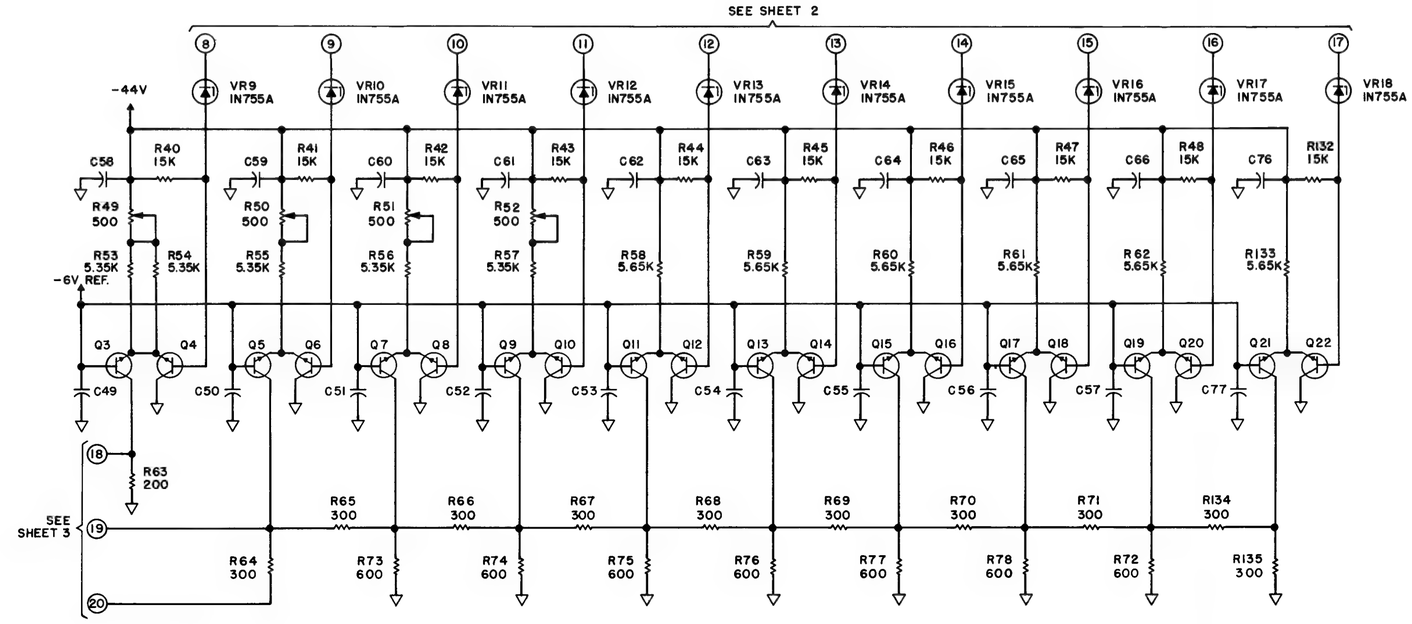
NOTE: RESISTORS R92-R126 ARE 470 OHMS.



352D911-2B

Change 7 FO-54. Alternate A/D Converter Printed Circuit (352D877G01) Schematic Diagram (Sheet 2 of 4)


SEE SHEET 1
-5.2V
R88 470
R39 470
C27
U27A 10505
R8 200
R10 200
U27B 10505
SEE SHEET 2
U26A MC1268
C26
C35
+5V
IBI
SEE SHEET 1
+12V
CR3 IN4148
R13 51 0.5W
C41
R12 1K
C67 22PF
Q2
T1
C68 10PF
R86 120
R87 120
R22 200 1W
C48
VR7 IN753A
VR5 IN753A
VR6 IN753A
U28 AM6853IU
R23 51
C28
-12 V
R21 200 1W
VR8 IN751A
SEE ASSEMBLY DETAIL REFER TO 352D877
T2
SEE SHEET 4
ENLARGED DETAIL
TRANSFORMER T2
R130 1K
C42
C29
TP1
R14 1K
Ø ON A
A17
R127 75
SYSTEM VIDEO A (COAX) IN
A11
A12
A/D TST 10
B (COAX) IN
A5
400HZ BITE SINE WAVE FROM 11T1-5
A6
R128 75
(NC)
A19
U29 DG188AA
IN VCC V2
DI
VR
D2
NC
SI
S2
VEE
R131 1K
C43
U30 LH0033G
R15 100
C44
C45 0.01
R16 100
C46 0.01
C30
CR5
CR7
CR4
CR6
TP2
R17 100
C69 150PF
U31 LH0033G
C47
R20 1K
TP3
R19 10
C31
R18 100
352D911-3B

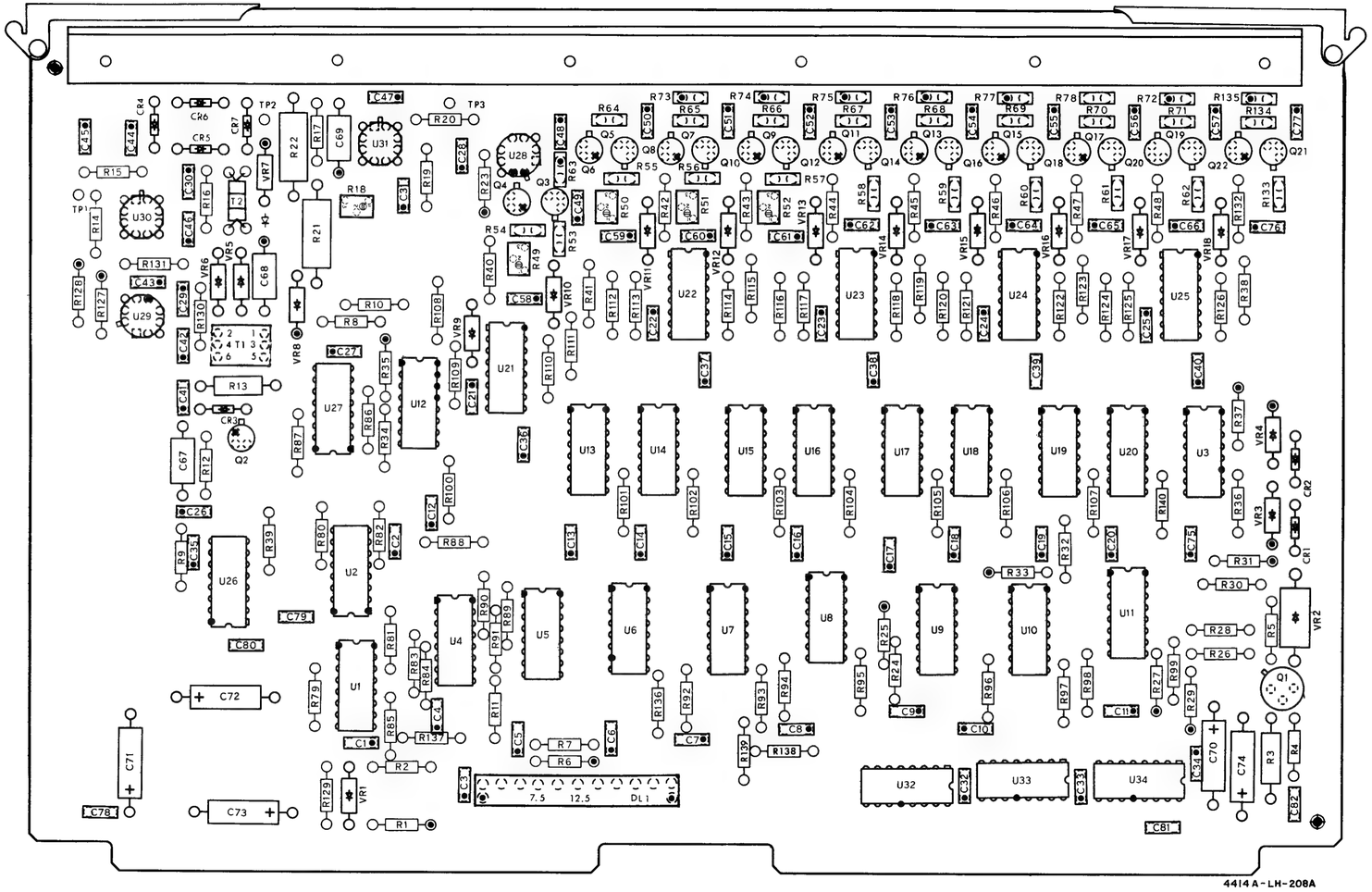


NOTES:

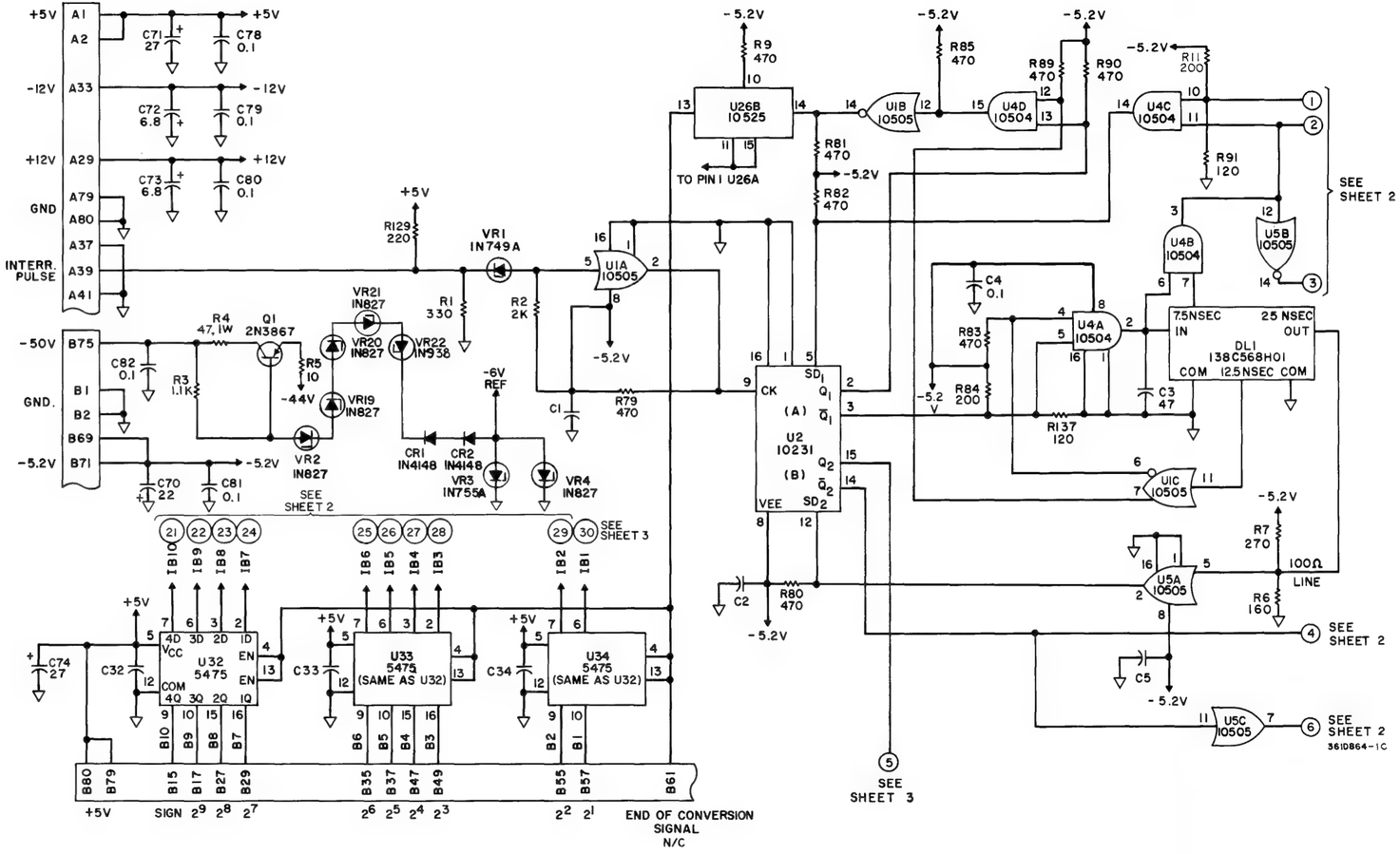
1. ALL EVEN NO. TRANSISTORS ARE 2N3227.
2. RESISTORS R92-R126 ARE 470 OHMS
3. C4-C44 & C47-C66 & C75-C82 ARE 0.1 MICROFARADS. C45, C46 ARE 0.01 MICROFARADS.
4. ALL RESISTANCE VALUES ARE IN OHMS
5. UNLESS STATED OTHERWISE GROUND ALL UNUSED PINS.
6. CR4 & CR5 ARE MATCHED PAIR 128C931H03 CR6 & CR7 ARE MATCHED PAIR 128C931H03
7. U1, U5, U9, U27 ARE PART NO. 581R688H07
8. U2, U6, U7, U8, U10, U11 ARE PART NO. 138C439H01
9. U3, & U12 TO U20 ARE PART NO. 138C566H01
10. U4 IS PART NO. 581R688H08
11. U21-U26 ARE PART NO. 138C461H01
12. U28 IS PART NO. 581R709H02
13. U29 IS PART NO. 578R823H03
14. U30, U31 ARE PART NO. 581R684H01
15. U32, U33, U34 ARE PART NO. 578R644H02
16. R58 TO R62 & R133 ARE PART NO. 128C885H25
17. R53 TO R57 ARE PART NO. 128C885H24
18. R63 IS PART NO. 128C885H29
19. R64 TO R71, R134, R135 ARE PART NO. 128C885H30
20. Q3, Q5, Q7, Q9, Q11, Q13, Q15, Q17, Q19, Q21 ARE PART NO. 578R796H02
21. T1 IS PART NO. 128C510H02

352D911-4A

FO-54. Alternate A/D Converter Printed Circuit (352D877G01) Schematic Diagram (Sheet 4 of 4)

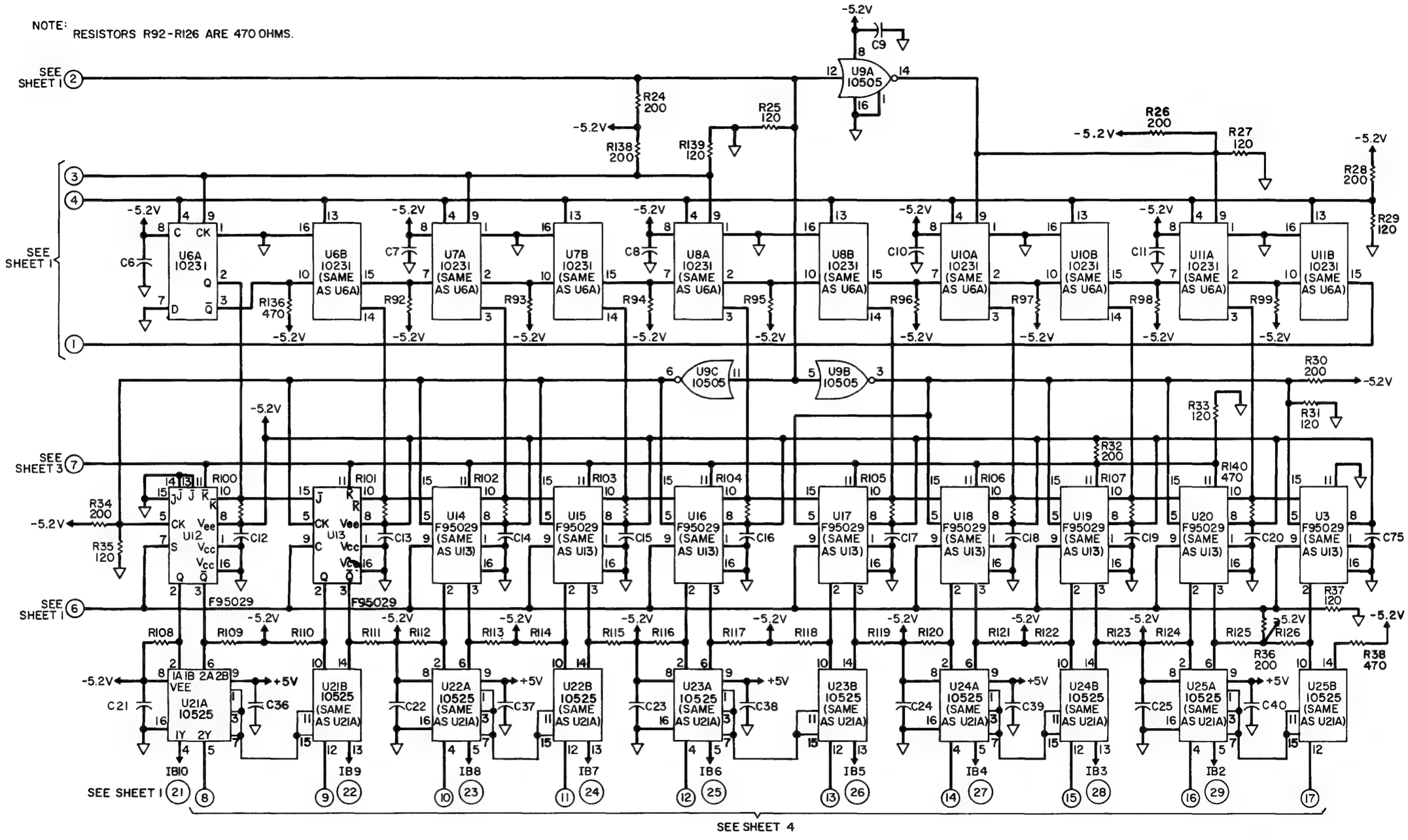


Change 7 FO-54.1. Alternate A/D Converter Printed Circuit (352D877G01) Board Component Layout

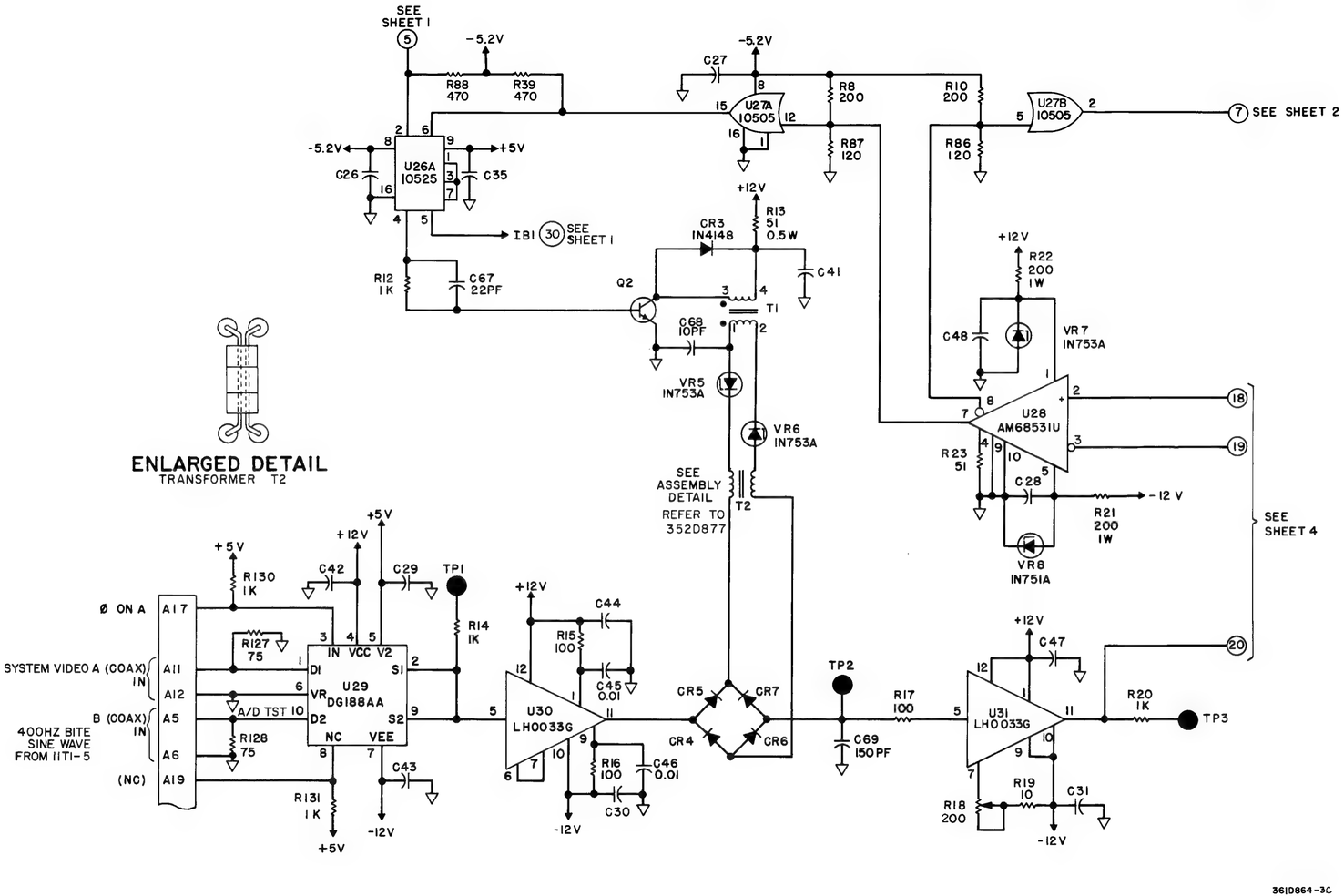


SEE NOTES ON SHEET 4

Change 7 FO-54.2. Ⓟ A/D Converter Printed Circuit (361D866G01) Schematic Diagram (Sheet 1 of 4)

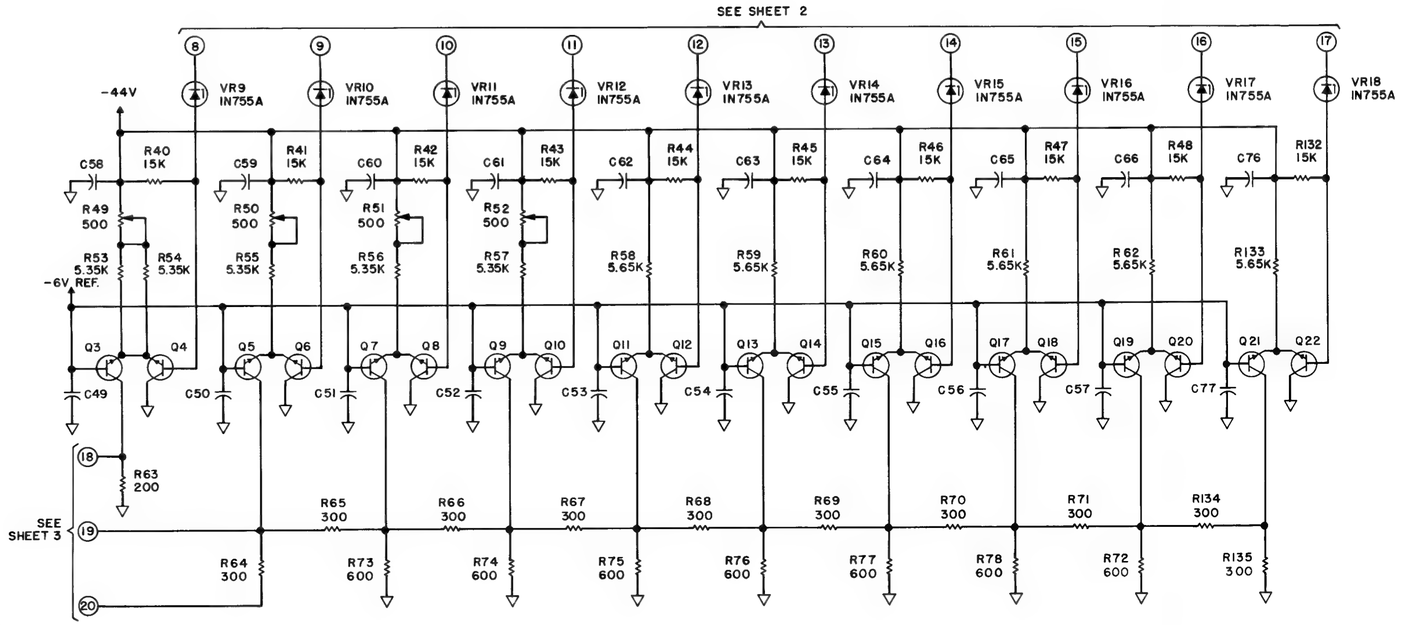


Change 7 FO-54.2. Ⓟ A/D Converter Printed Circuit (361D866G01) Schematic Diagram (Sheet 2 of 4)



361D864-3C

Change 7 FO-54.2. (P) A/D Converter Printed Circuit (361D866G01) Schematic Diagram (Sheet 3 of 4)



NOTES:

1. ALL EVEN NO. TRANSISTORS ARE 2N3227.
2. RESISTORS R92–R126 ARE 470 OHMS
3. C4-C44 & C47-C66 & C75-C82 ARE 0.1 MICROFARADS. C45, C46 ARE 0.01 MICROFARADS.
4. ALL RESISTANCE VALUES ARE IN OHMS
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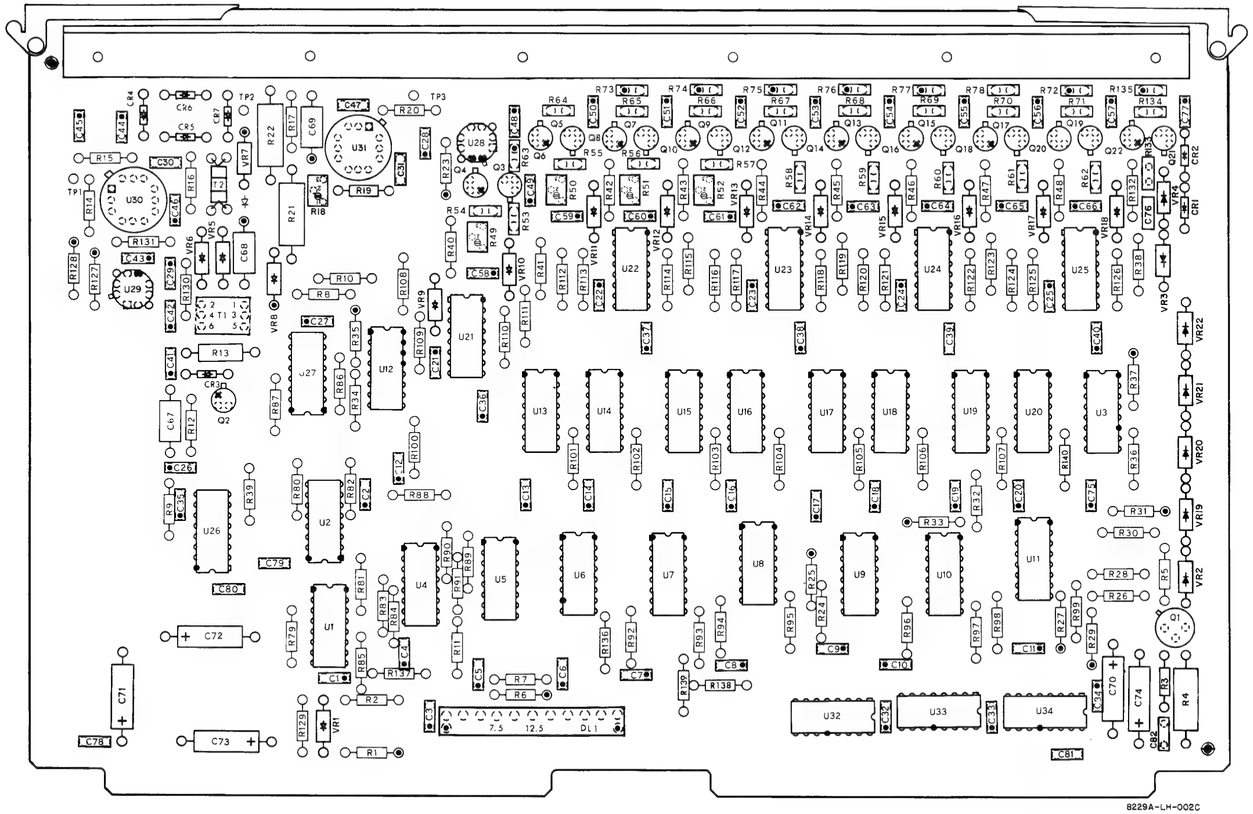
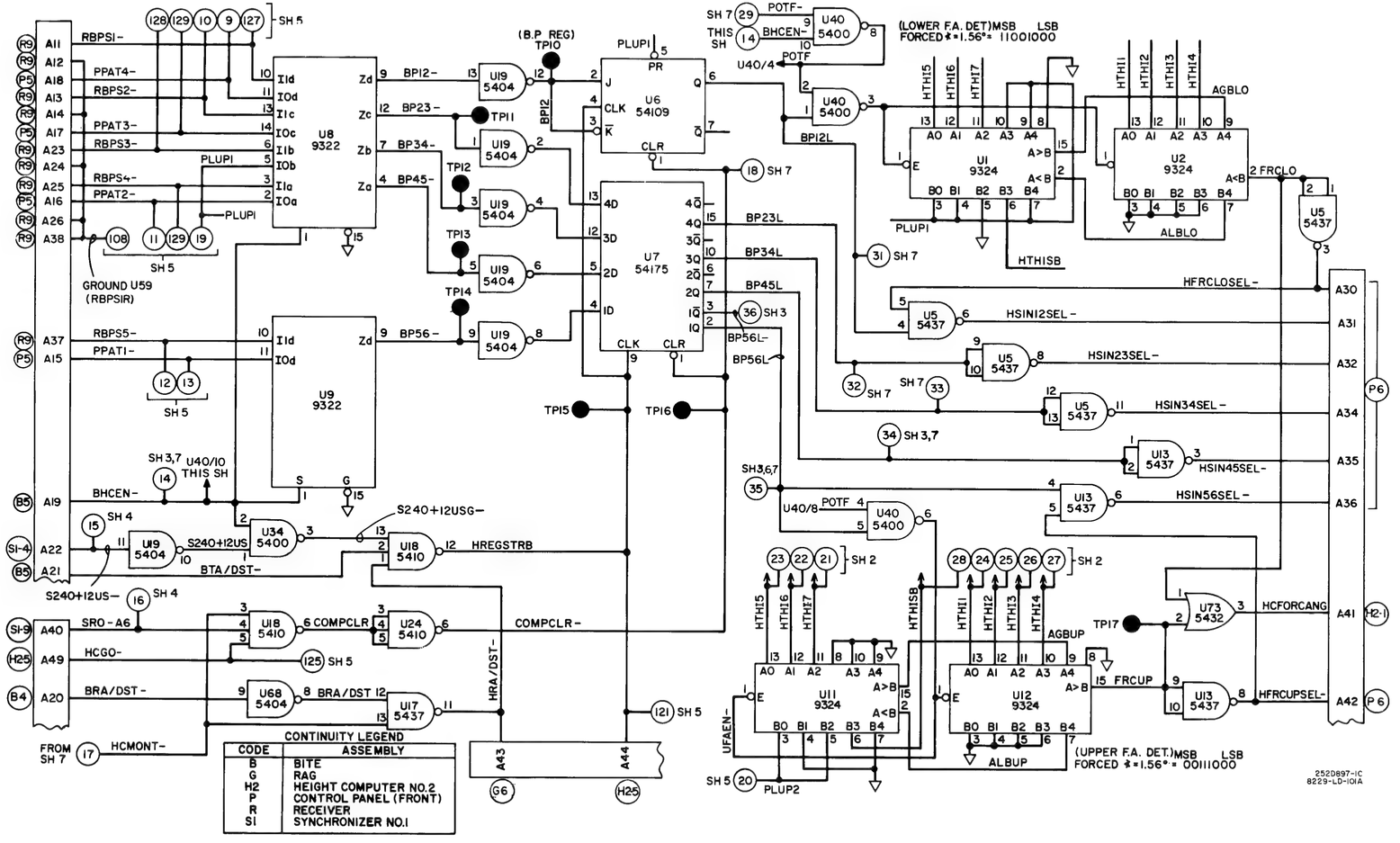
6. CR4 & CR5 ARE MATCHED PAIR 128C931H03 CR6 & CR7 ARE MATCHED PAIR 128C931H03
7. U1, U5, U9, U27 ARE PART NO. 581R688H07
8. U2, U6, U7, U8, U10, U11 ARE PART NO. 138C439H01
9. U3, & U12 TO U20 ARE PART NO. 138C566H01
10. U4 IS PART NO. 581R688H08
11. U21–U26 ARE PART NO. 583R357H02
12. U28 IS PART NO. 581R709H02
13. U29 IS PART NO. 578R823H03
14. U30, U31 ARE PART NO. 581R684H01
15. U32, U33, U34 ARE PART NO. 578R644H02
16. R58 TO R62 & R133 ARE PART NO. 128C885H25
17. R53 TO R57 ARE PART NO. 128C885H24
18. R63 IS PART NO. 128C885H29
19. R64 TO R71, R134, R135 ARE PART NO. 128C885H30
20. Q3, Q5, Q7, Q9, Q11, Q13, Q15, Q17, Q19, Q21 ARE PART NO. 578R796H02
21. T1 IS PART NO. 128C510H02

361D864-4

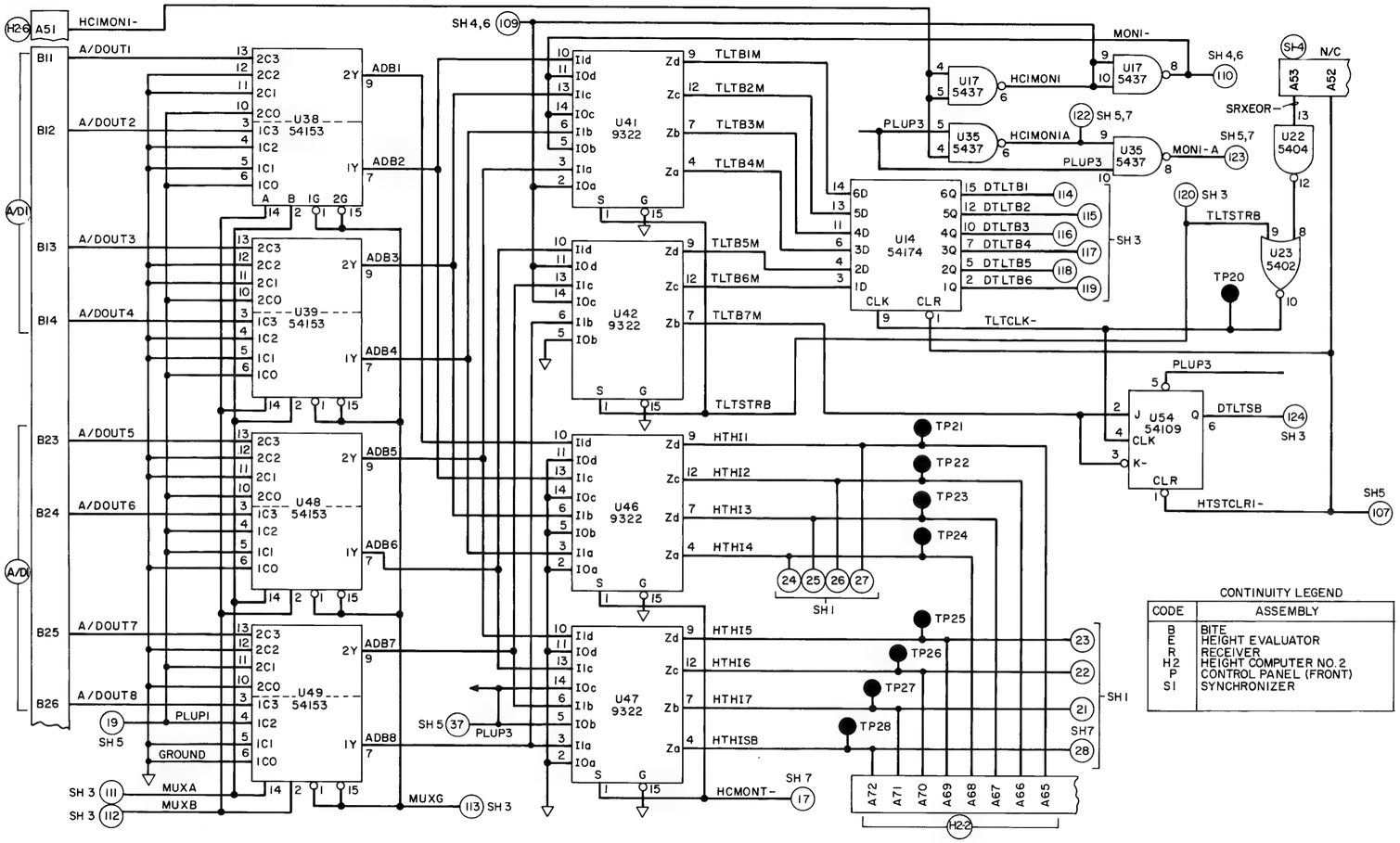
Change 7 FO-54.2. (P) A/D Converter Printed Circuit (361D866G01) Schematic Diagram (Sheet 4 of 4)



Change 7 FO-54.3. Ⓟ A/D Converter Printed Circuit (361D866G01) Board Component Layout



Change 7 FO-55. Height Computer No. 1 Planar Array (352D862) Logic Diagram (Sheet 1 of 7)



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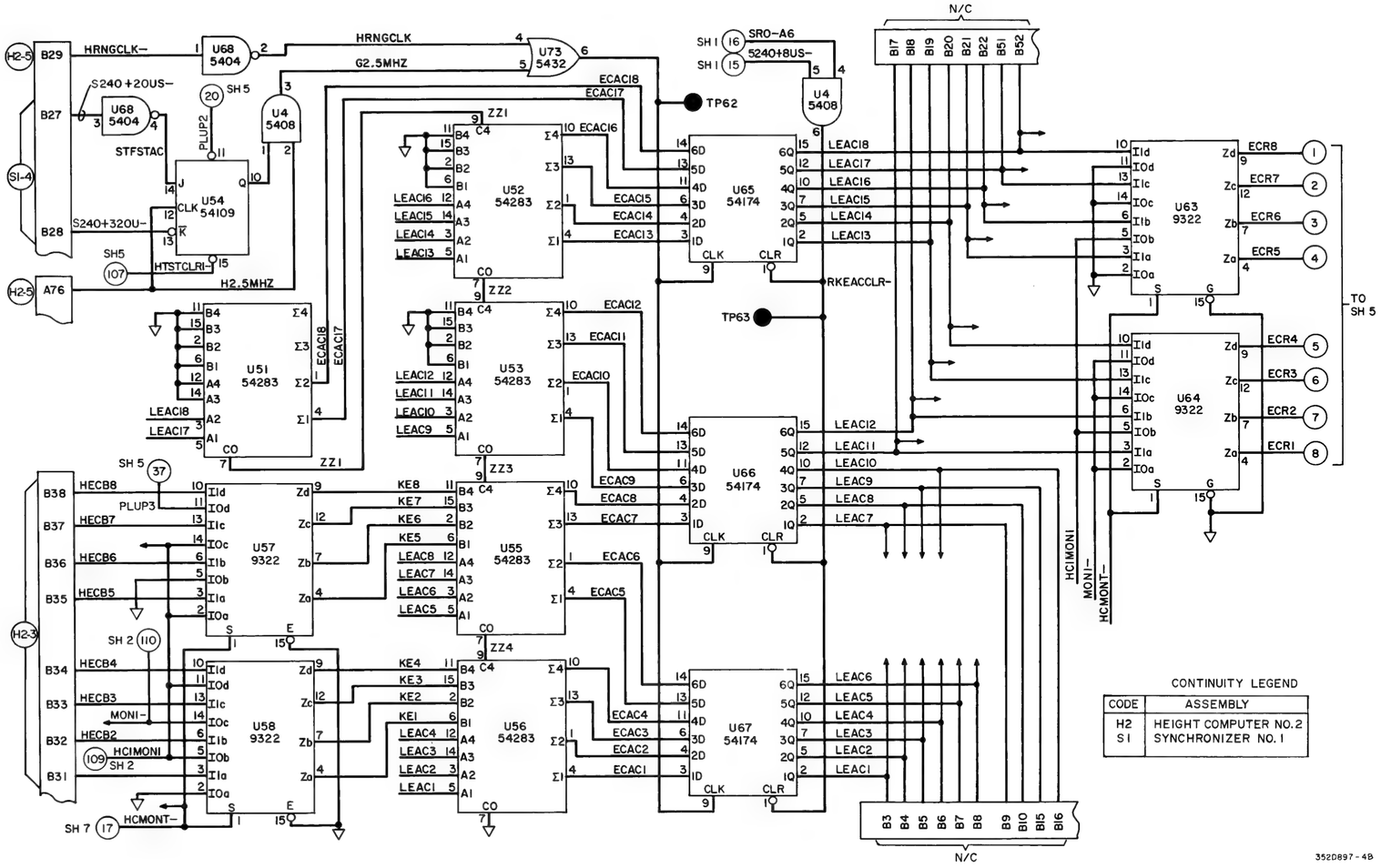
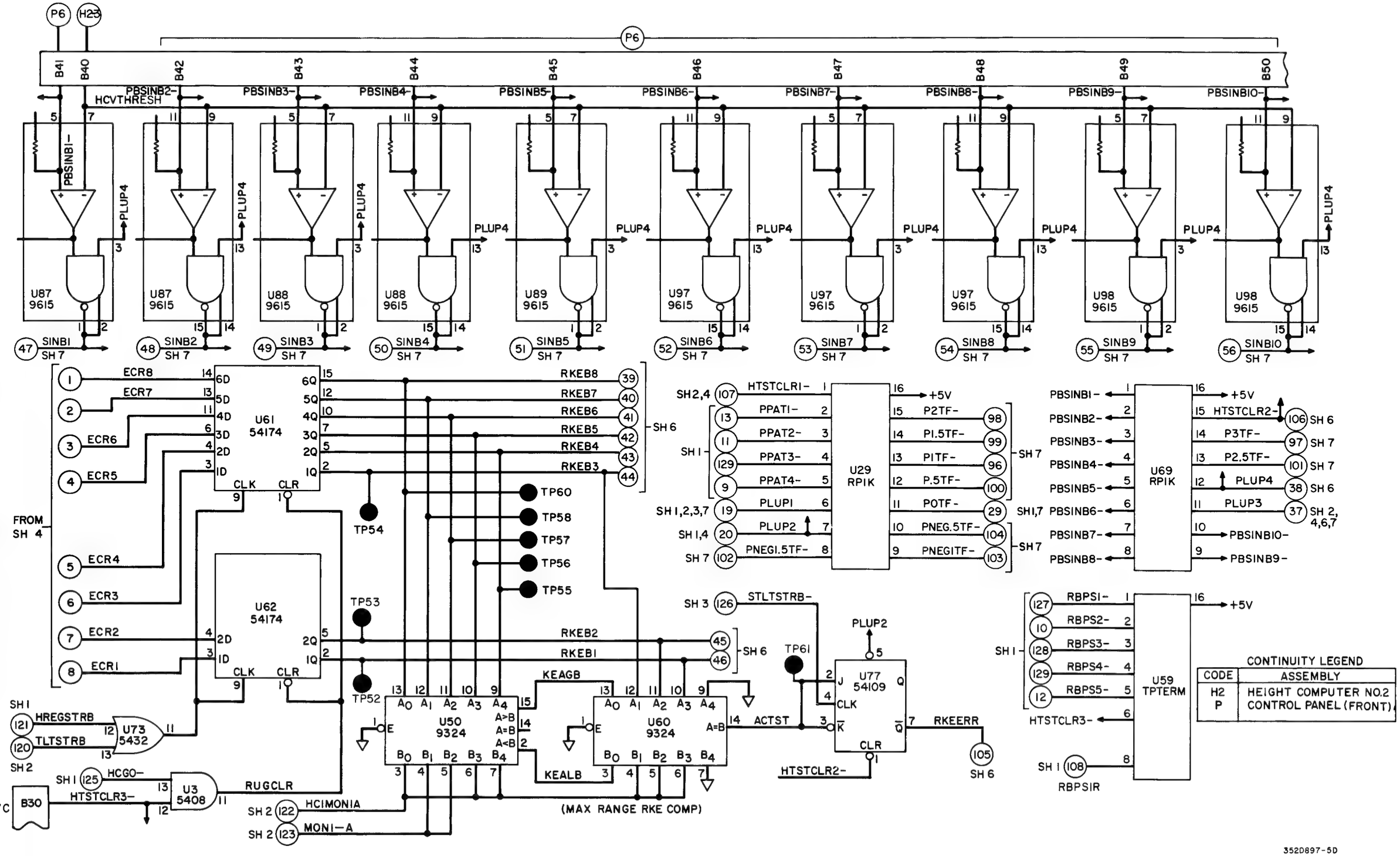
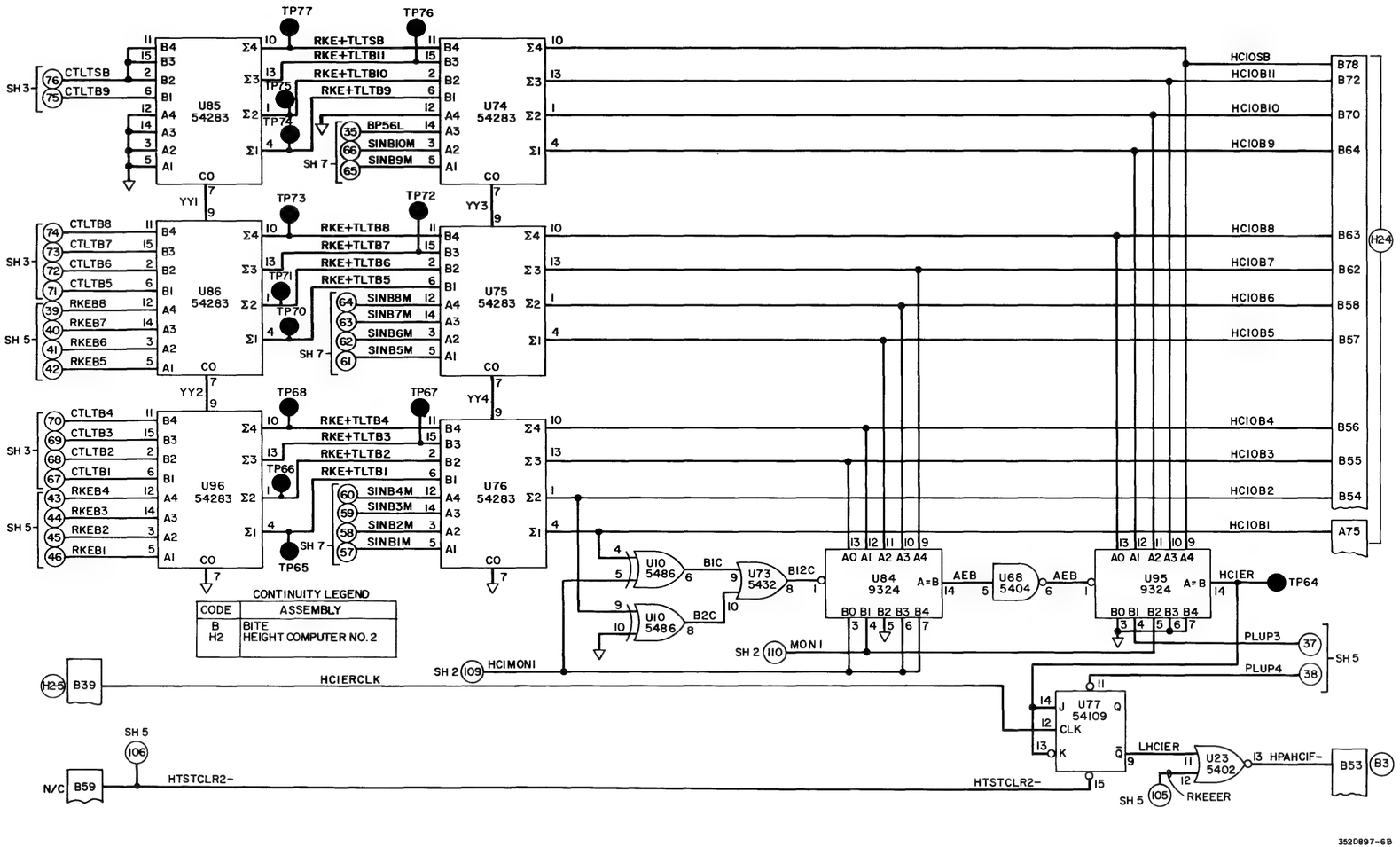
FO-55. Height Computer No. 1 Planar Array (352D862) Logic Diagram (Sheet 2 of 7)



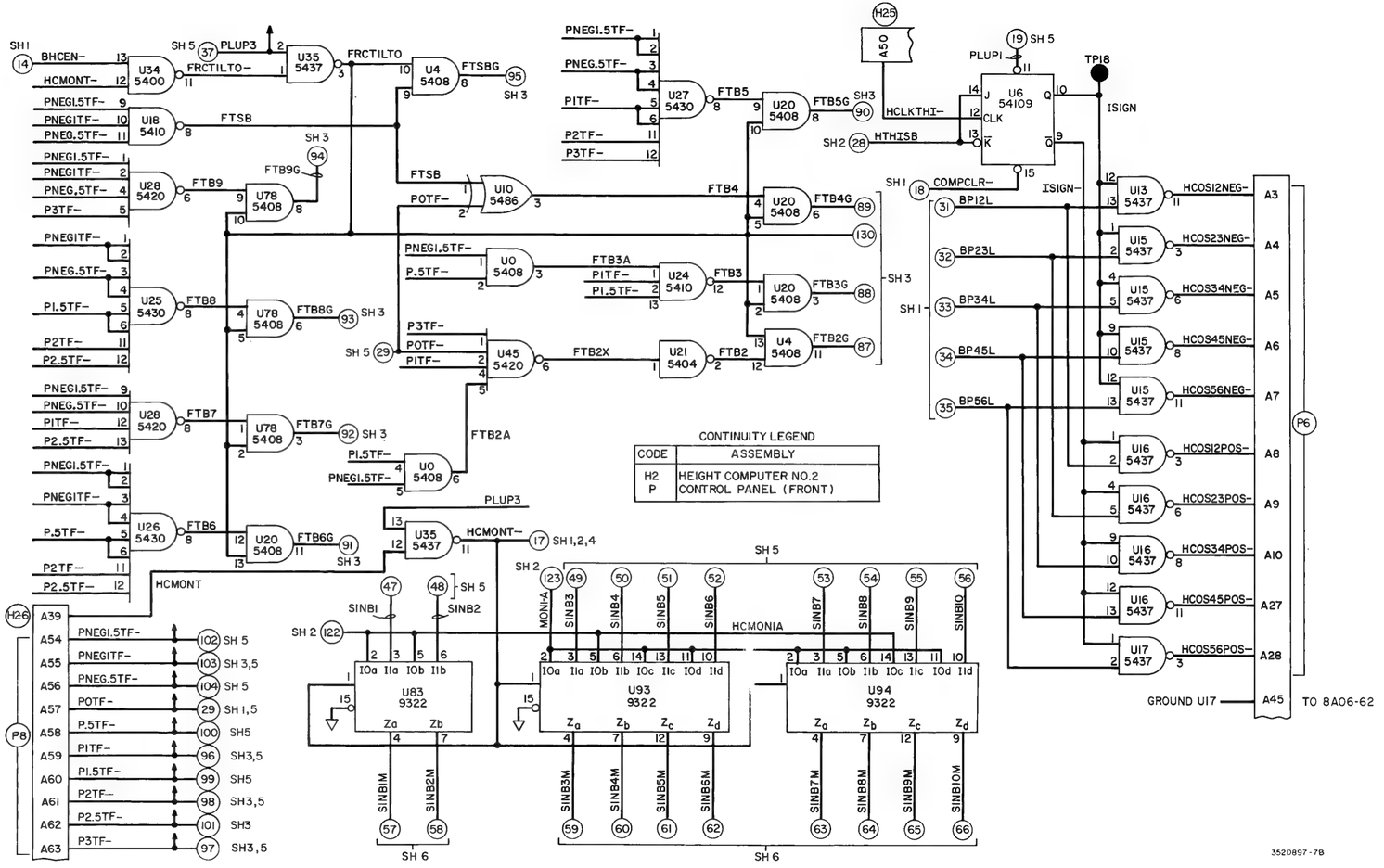
FO-55. Height Computer No. 1 Planar Array (352D862) Logic Diagram (Sheet 4 of 7)



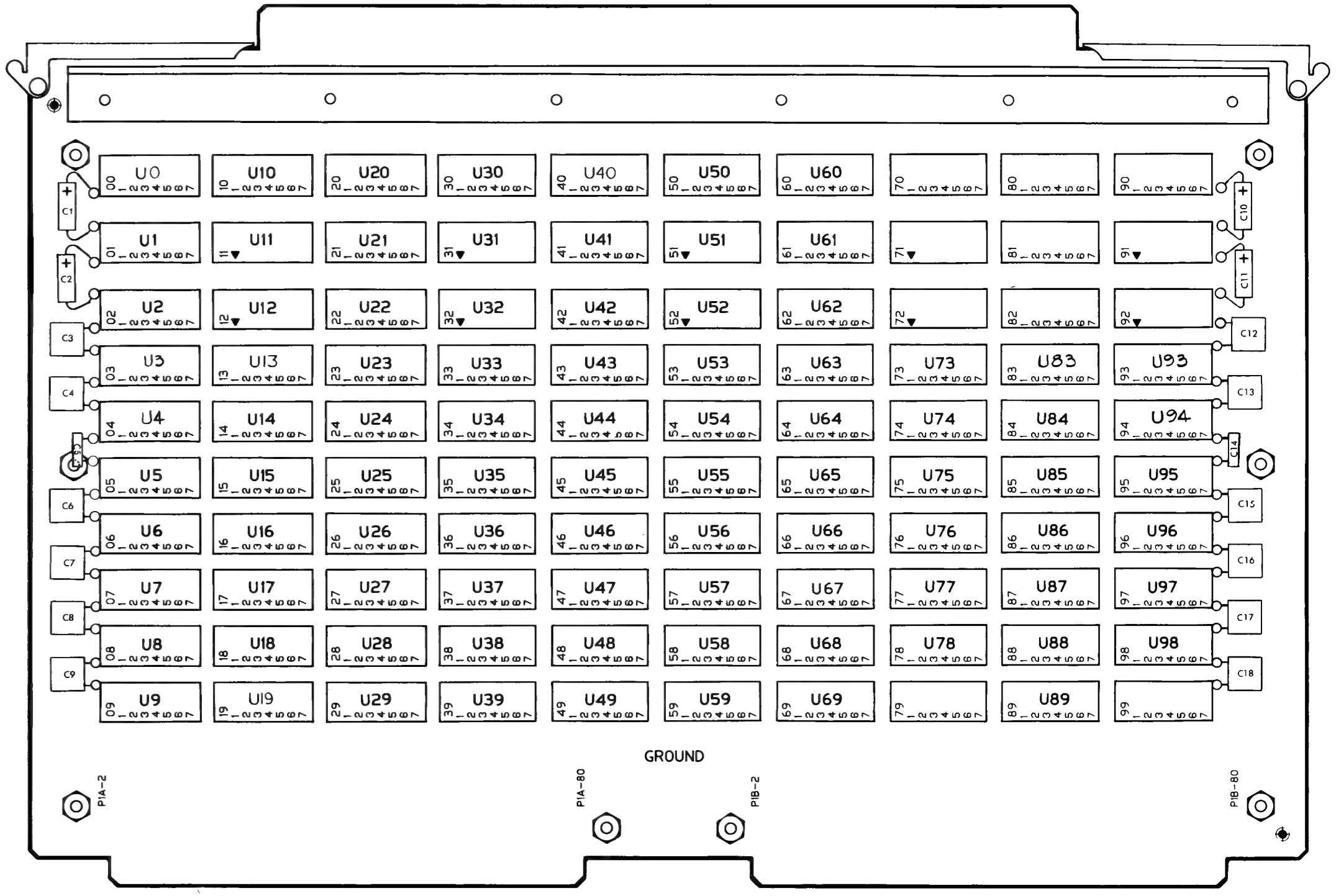
Change 7 FO-55. Height Computer No. 1 Planar Array (352D862) Logic Diagram (Sheet 5 of 7)



FO-55. Height Computer No. 1 Planar Array (352D862) Logic Diagram (Sheet 6 of 7)

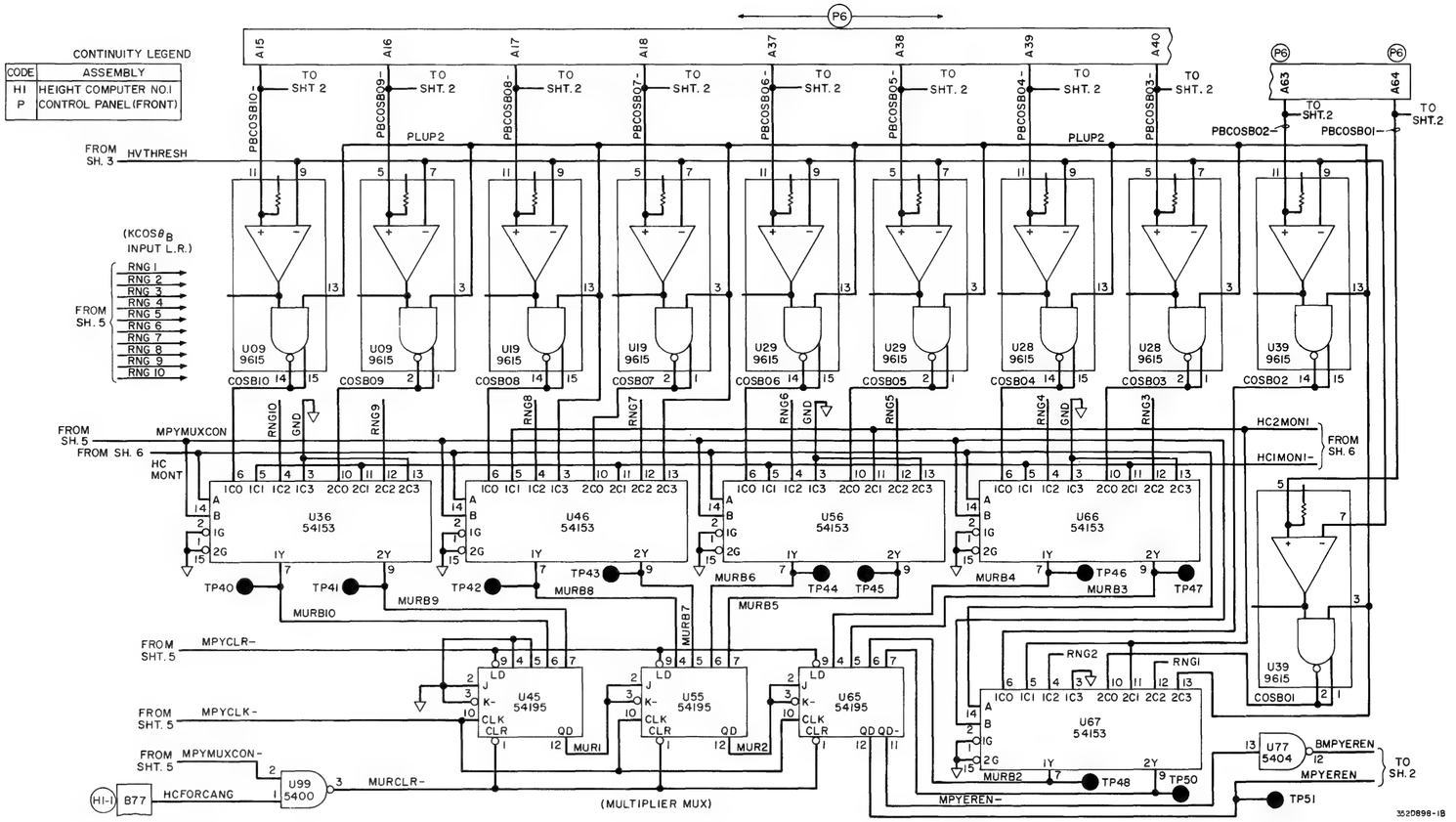


FO-55. Height Computer No. 1 Planar Array (352D862) Logic Diagram (Sheet 7 of 7)

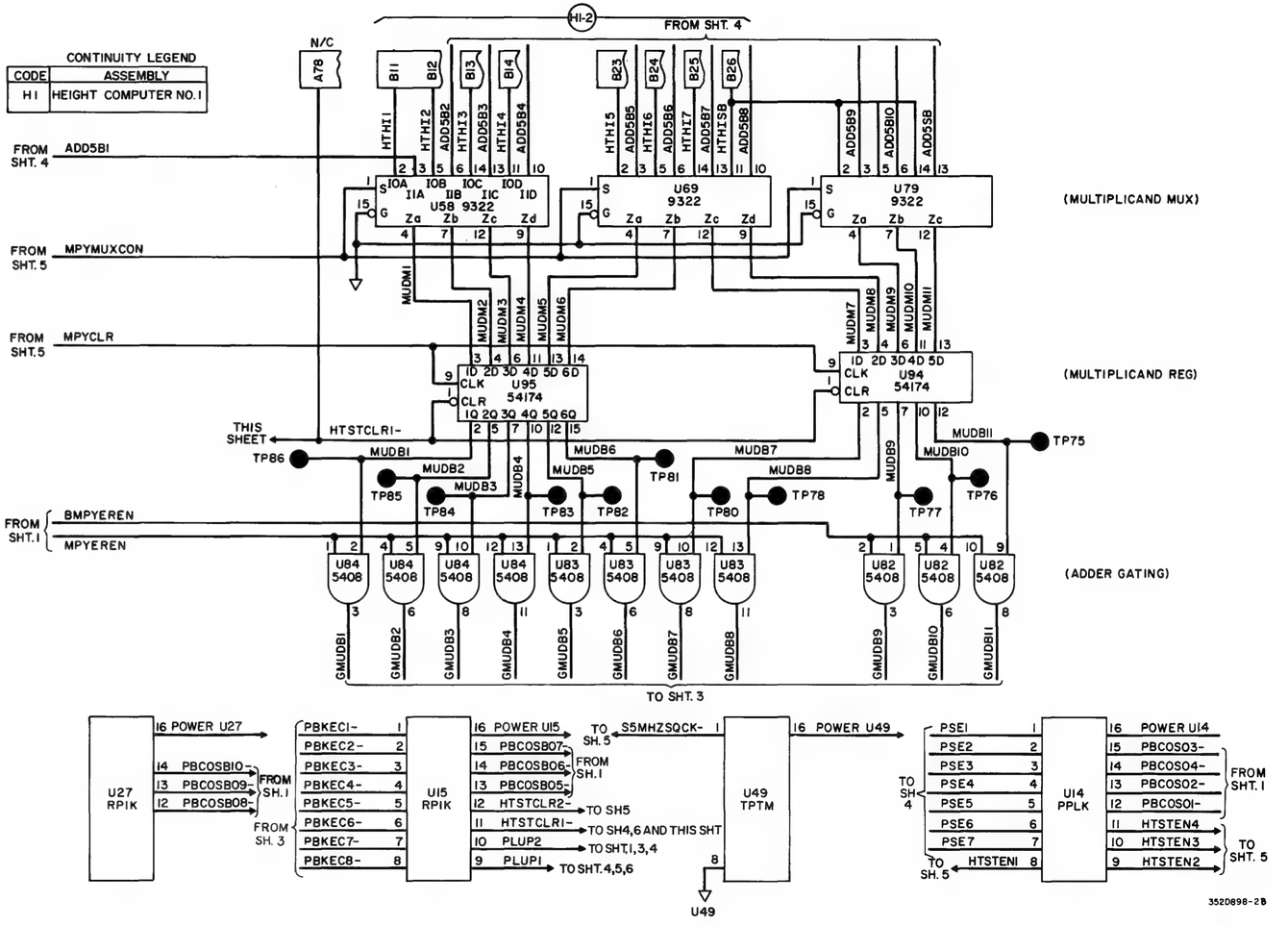


4414A-LD-209A

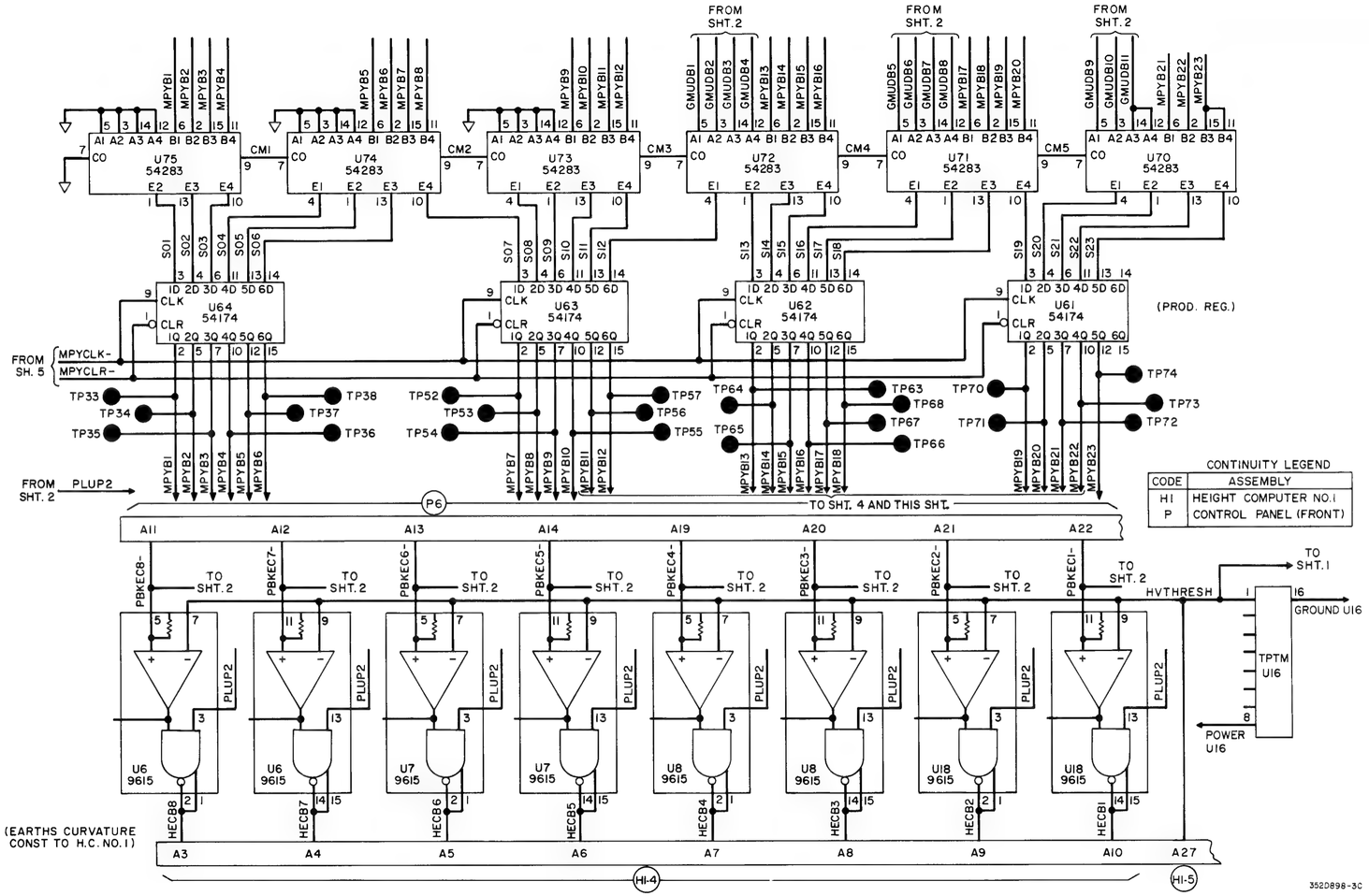
Change 1 FO-55.1 Height Computer No. 1 Planar Array (352D862) Board Component Layout



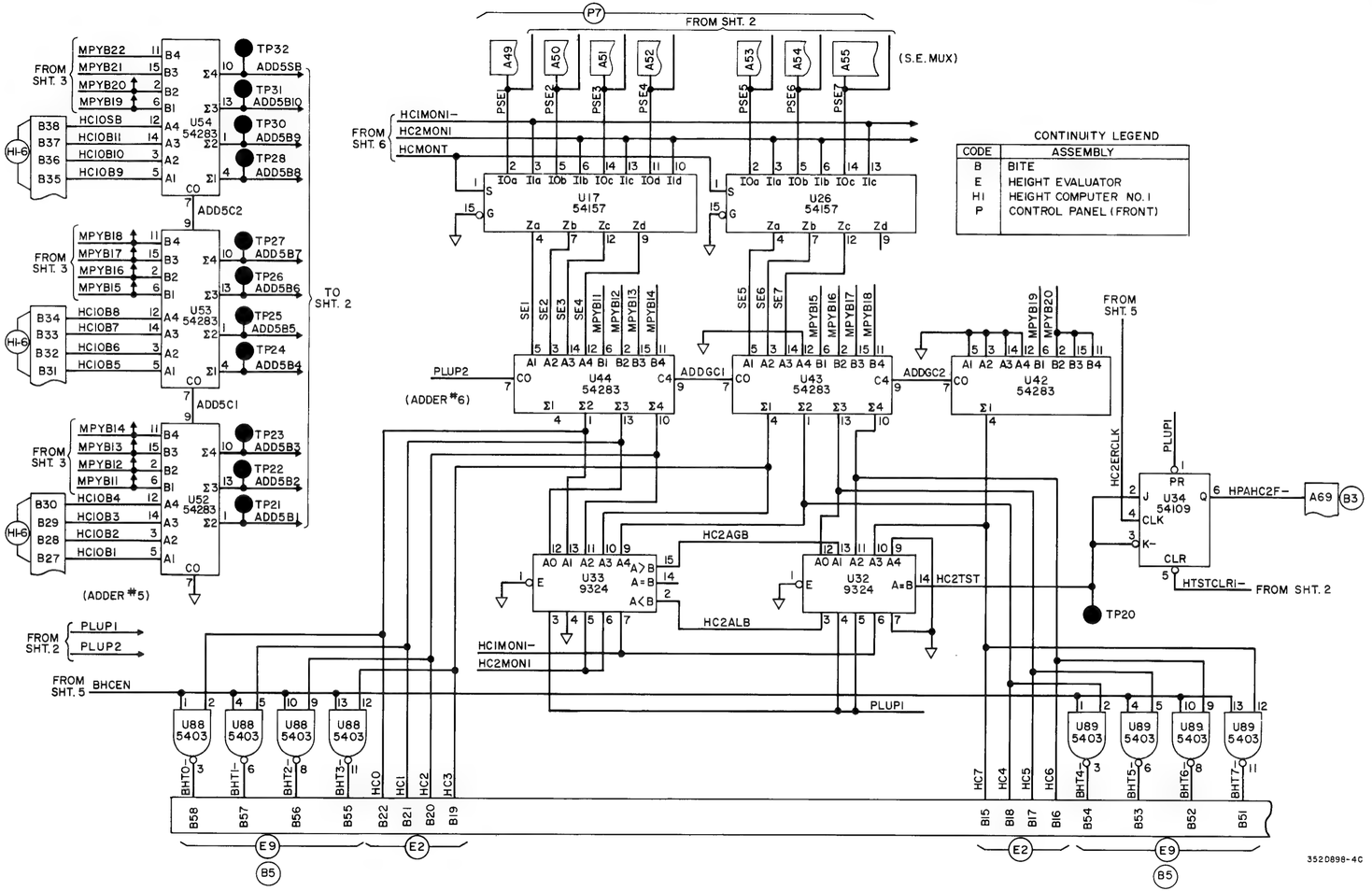
FO-56. Height Computer No. 2 Planar Array (352D863) Logic Diagram (Sheet 1 of 6)



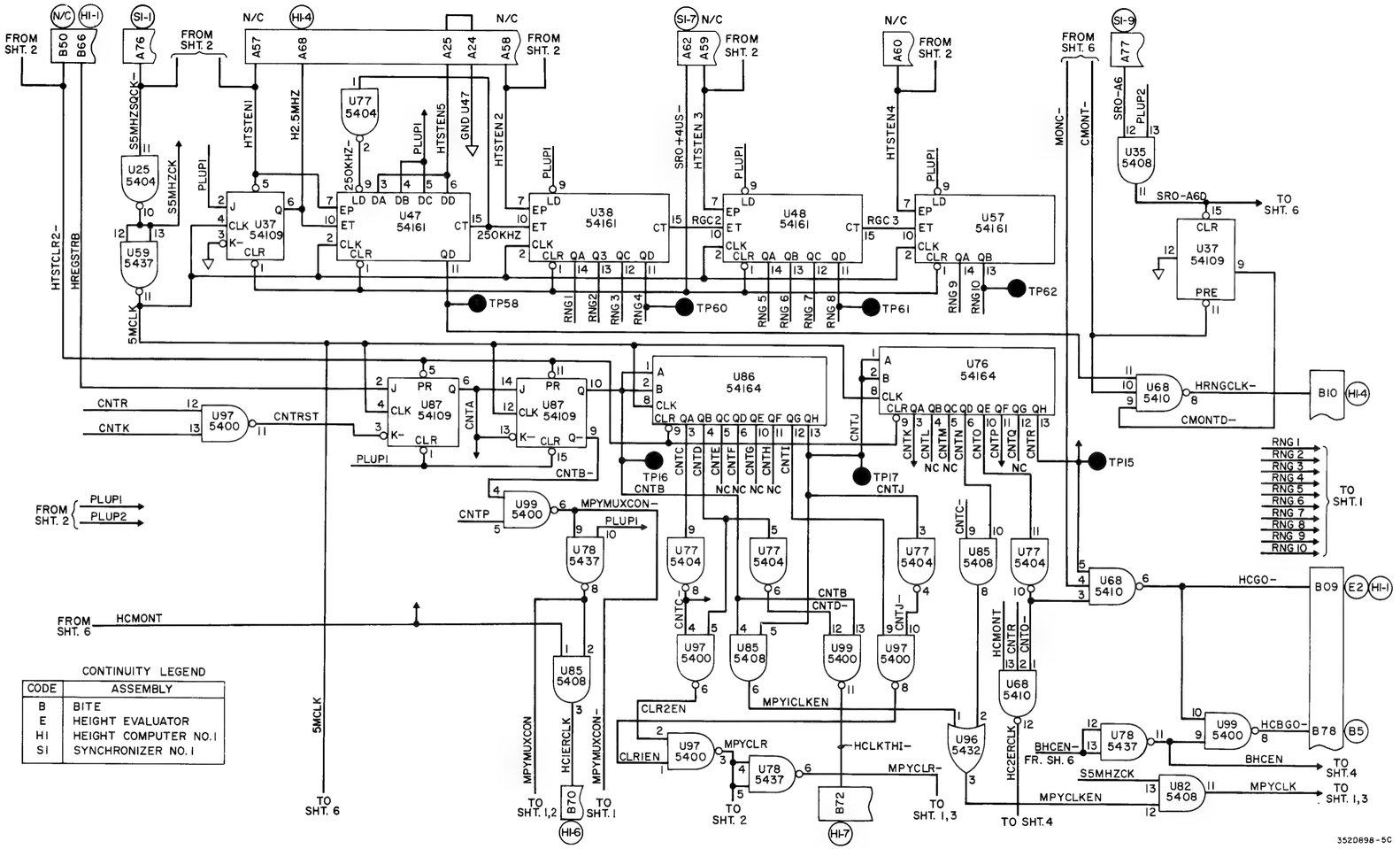
FO-56. Height Computer No. 2 Planar Array (352D863) Logic Diagram (Sheet 2 of 6)



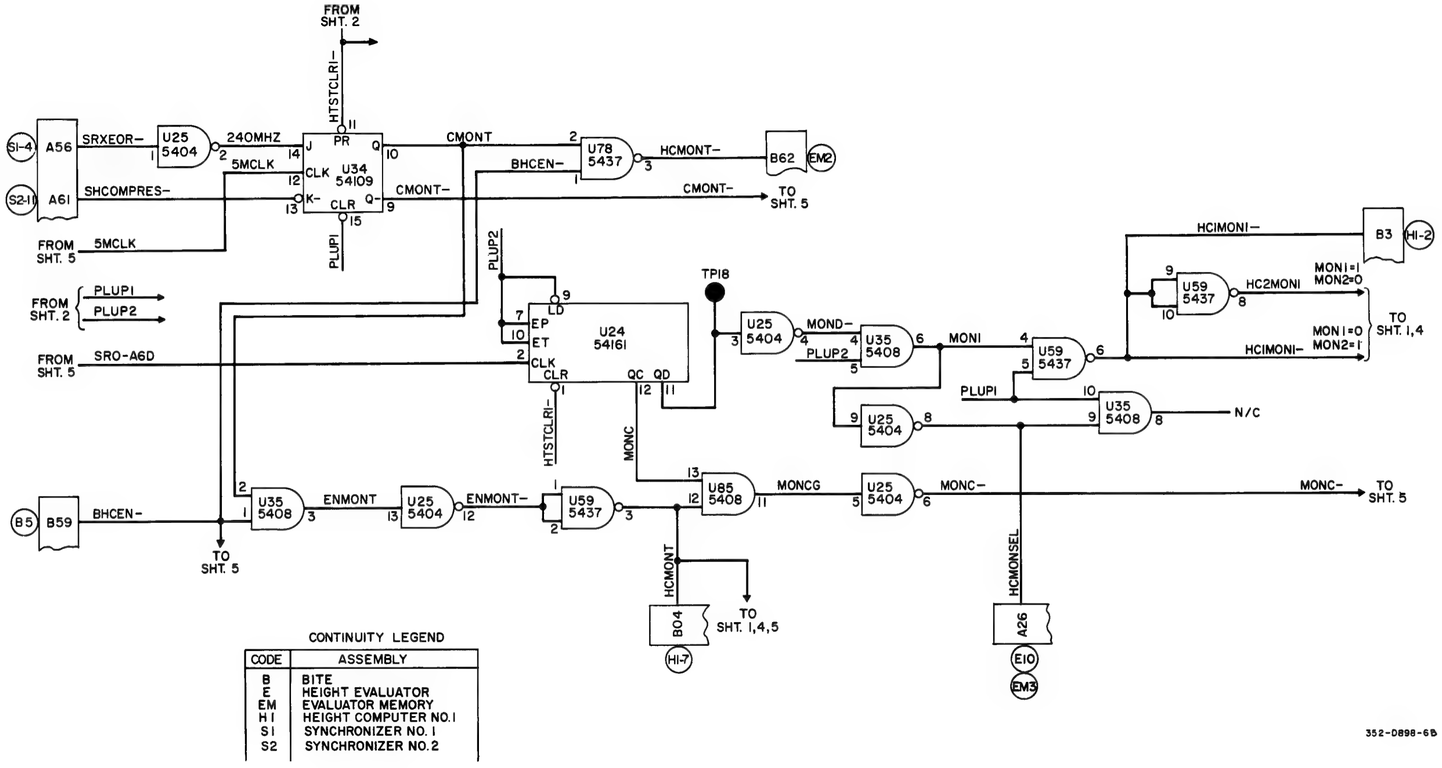
Change 7 FO-56. Height Computer No. 2 Planar Array (352D863) Logic Diagram (Sheet 3 of 6)



Change 7 FO-56. Height Computer No. 2 Planar Array (352D863) Logic Diagram (Sheet 4 of 6)



Change 7 FO-56. Height Computer No. 2 Planar Array (352D863) Logic Diagram (Sheet 5 of 6)

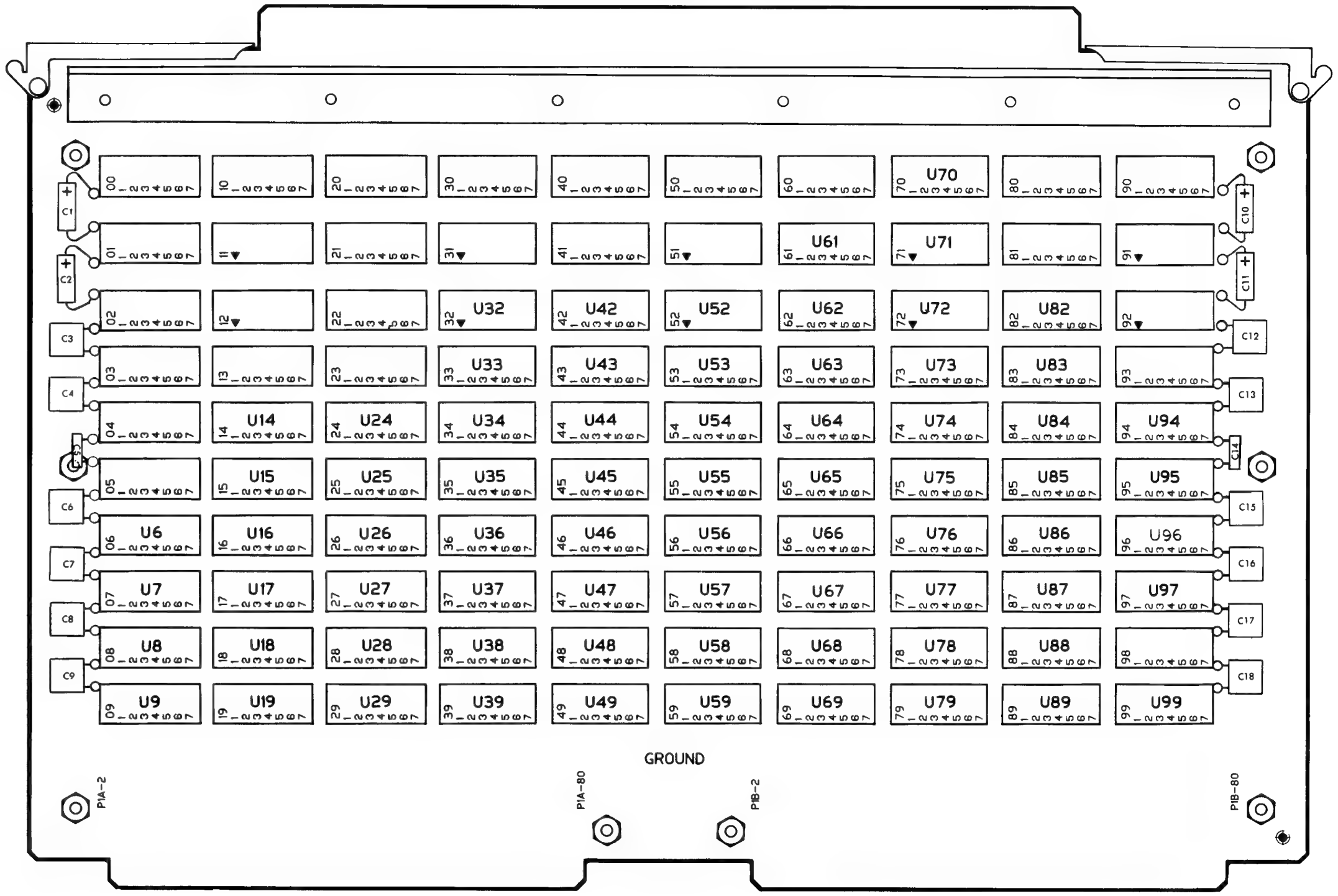


CONTINUITY LEGEND

CODE	ASSEMBLY
B	BITE
E	HEIGHT EVALUATOR
EM	EVALUATOR MEMORY
HI	HEIGHT COMPUTER NO.1
SI	SYNCHRONIZER NO. 1
S2	SYNCHRONIZER NO.2

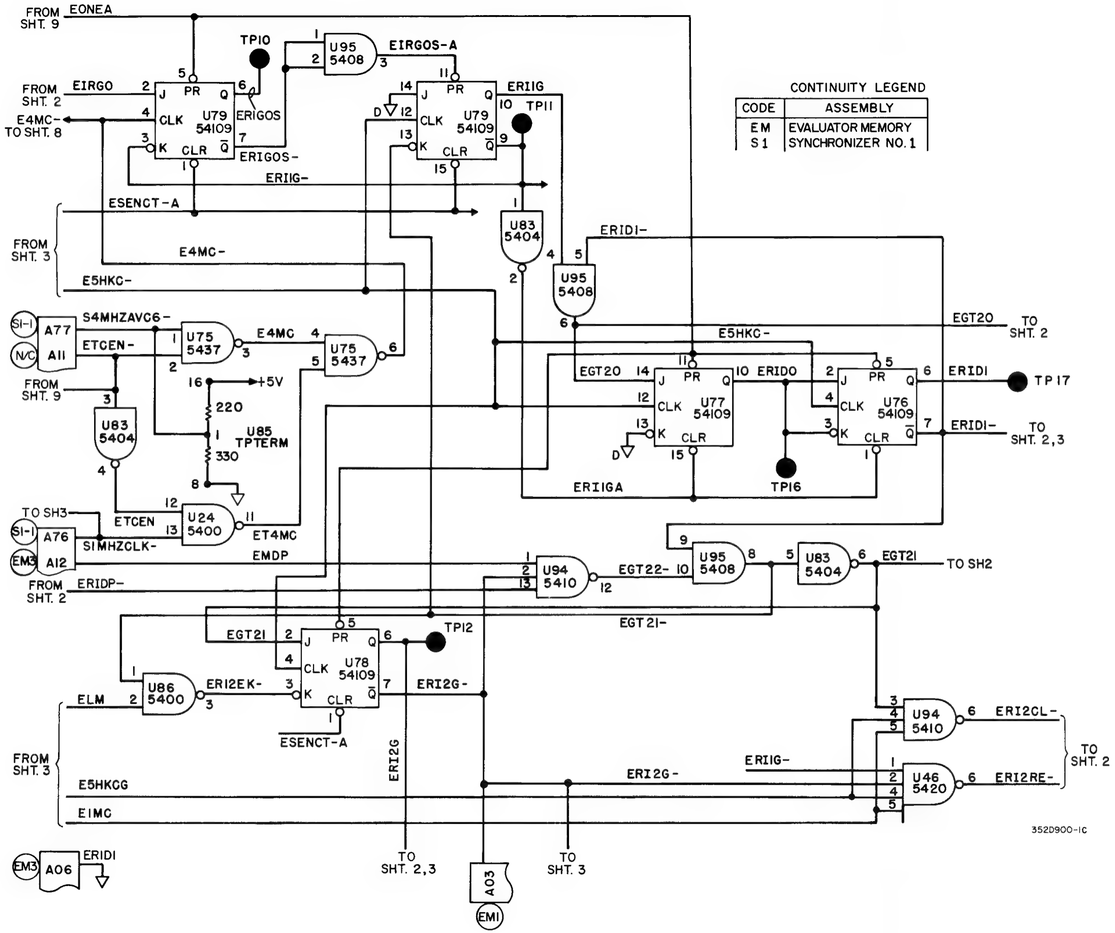
352-D898-6B

FO-56. Height Computer No. 2 Planar Array (352D863) Logic Diagram (Sheet 6 of 6)

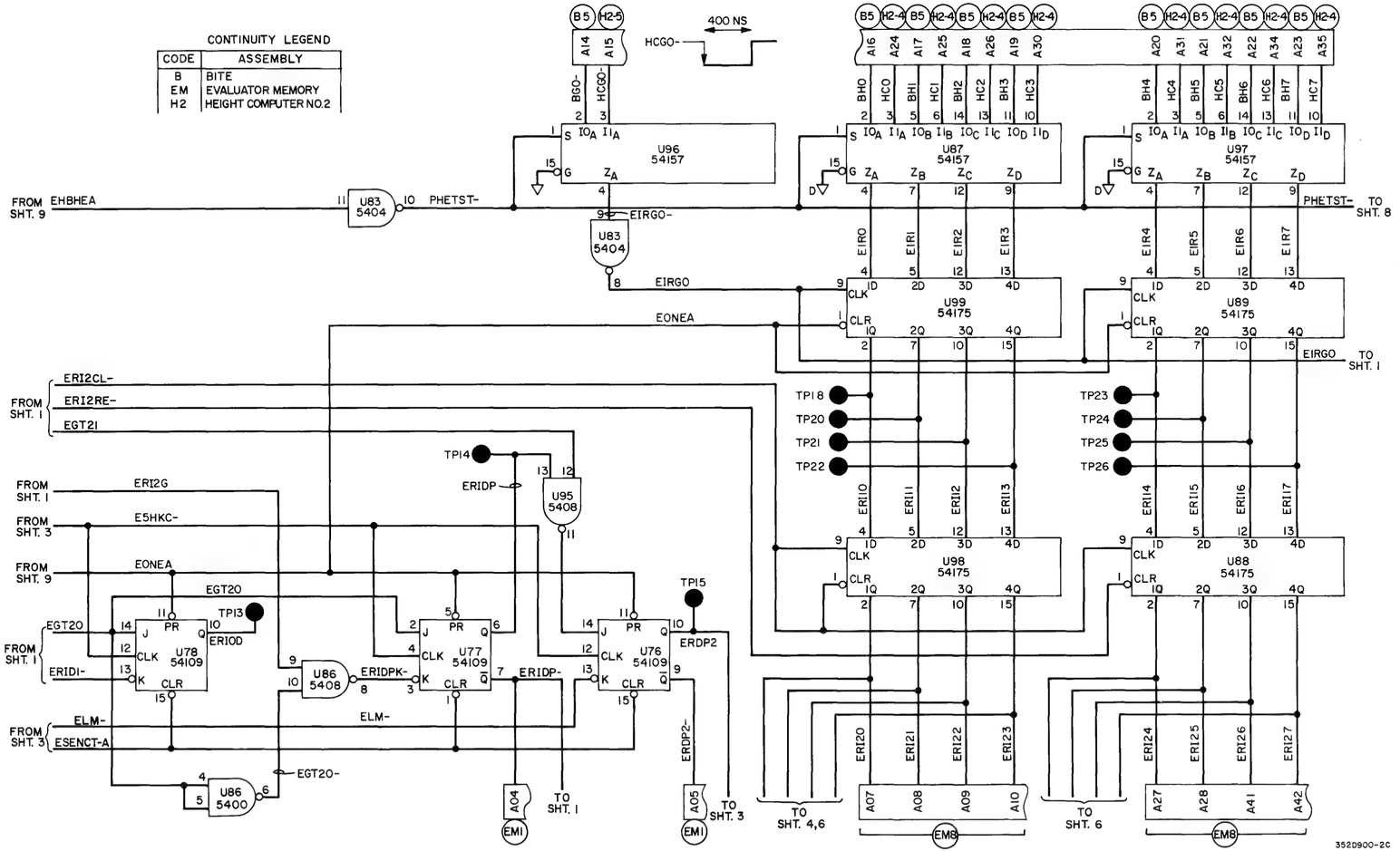


4414A-LD-210A

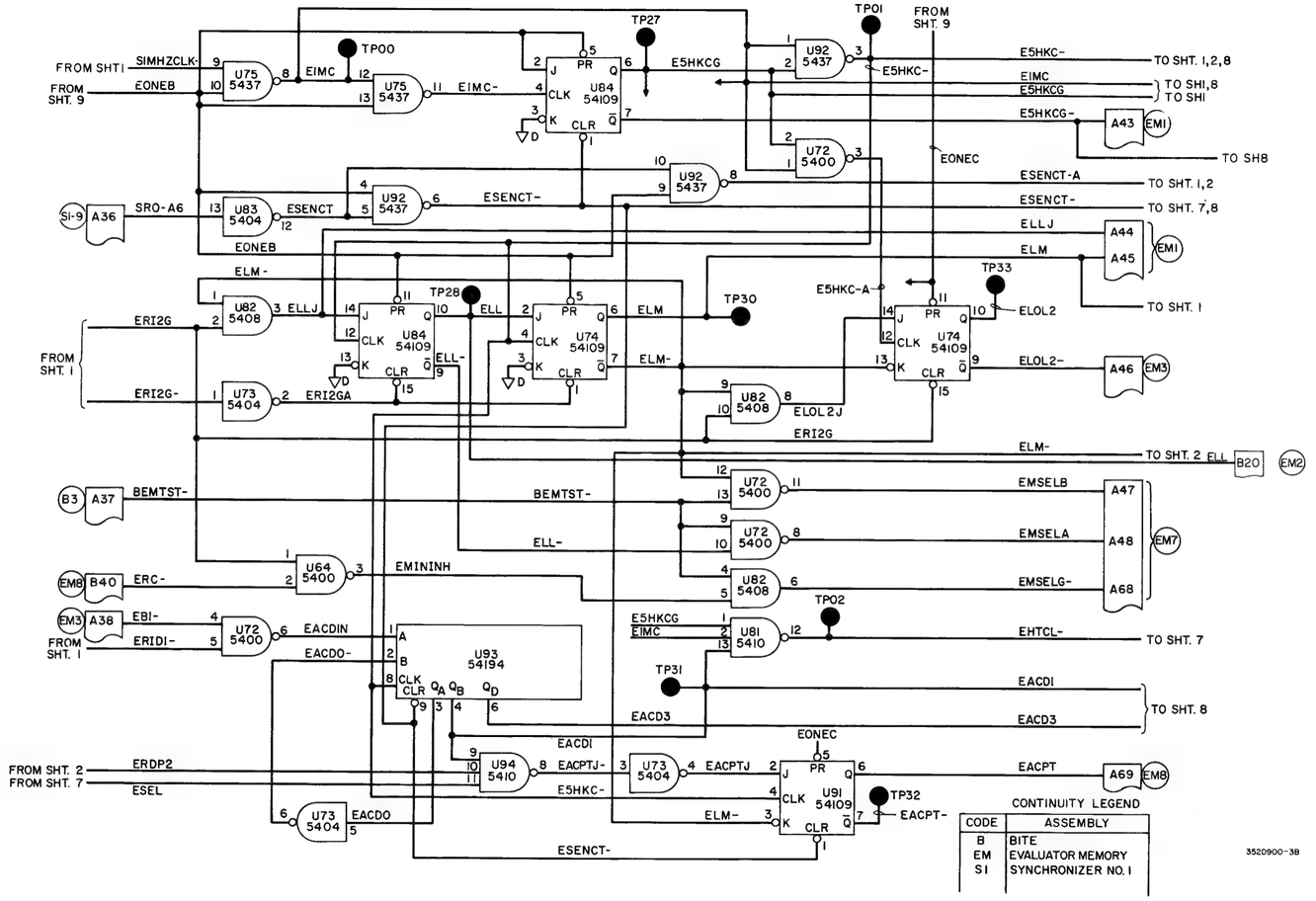
Change 1 FO-56.1 Height Computer No. 2 Planar Array (352D863) Board Component Layout



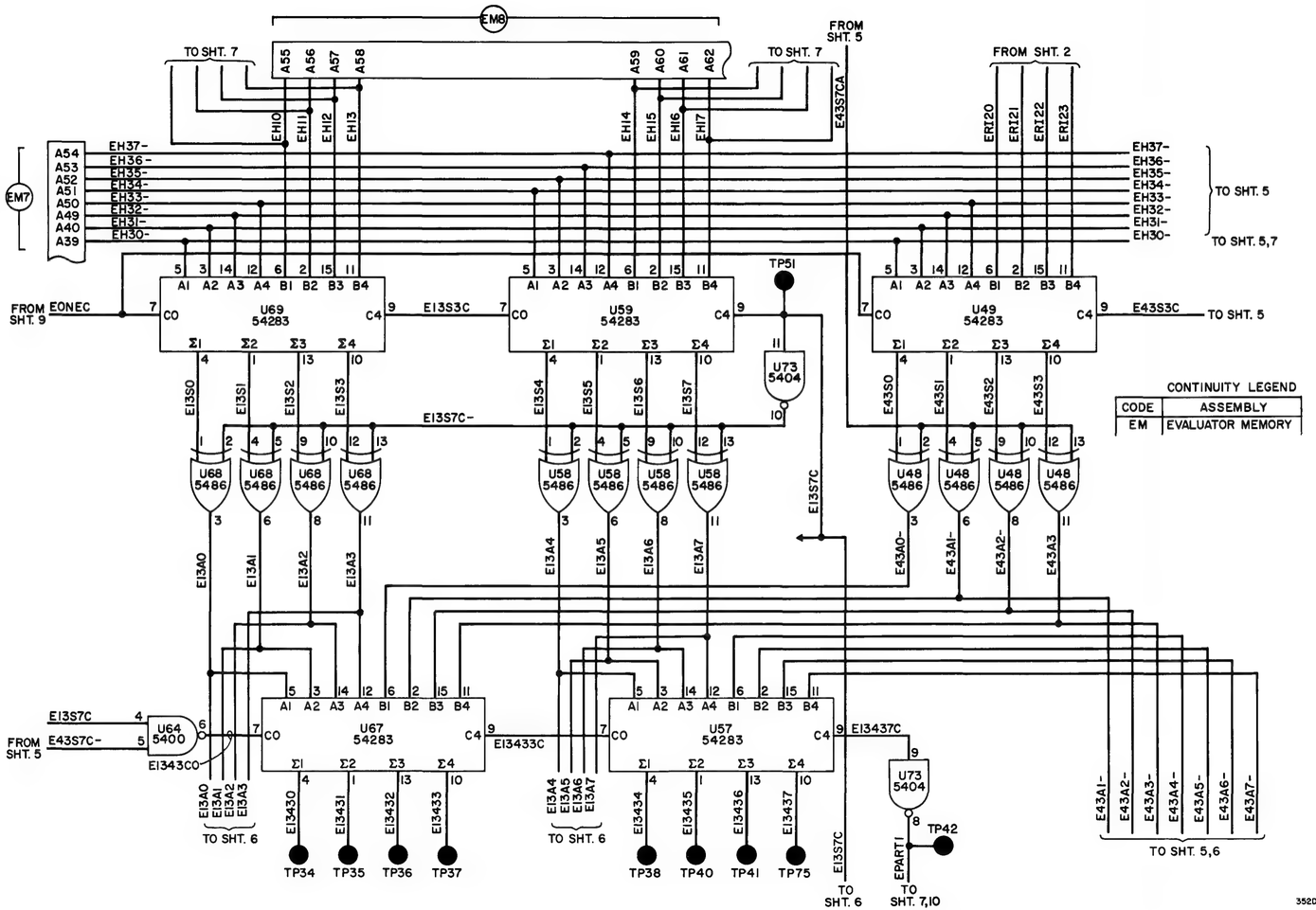
Change 7 FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 1 of 10)



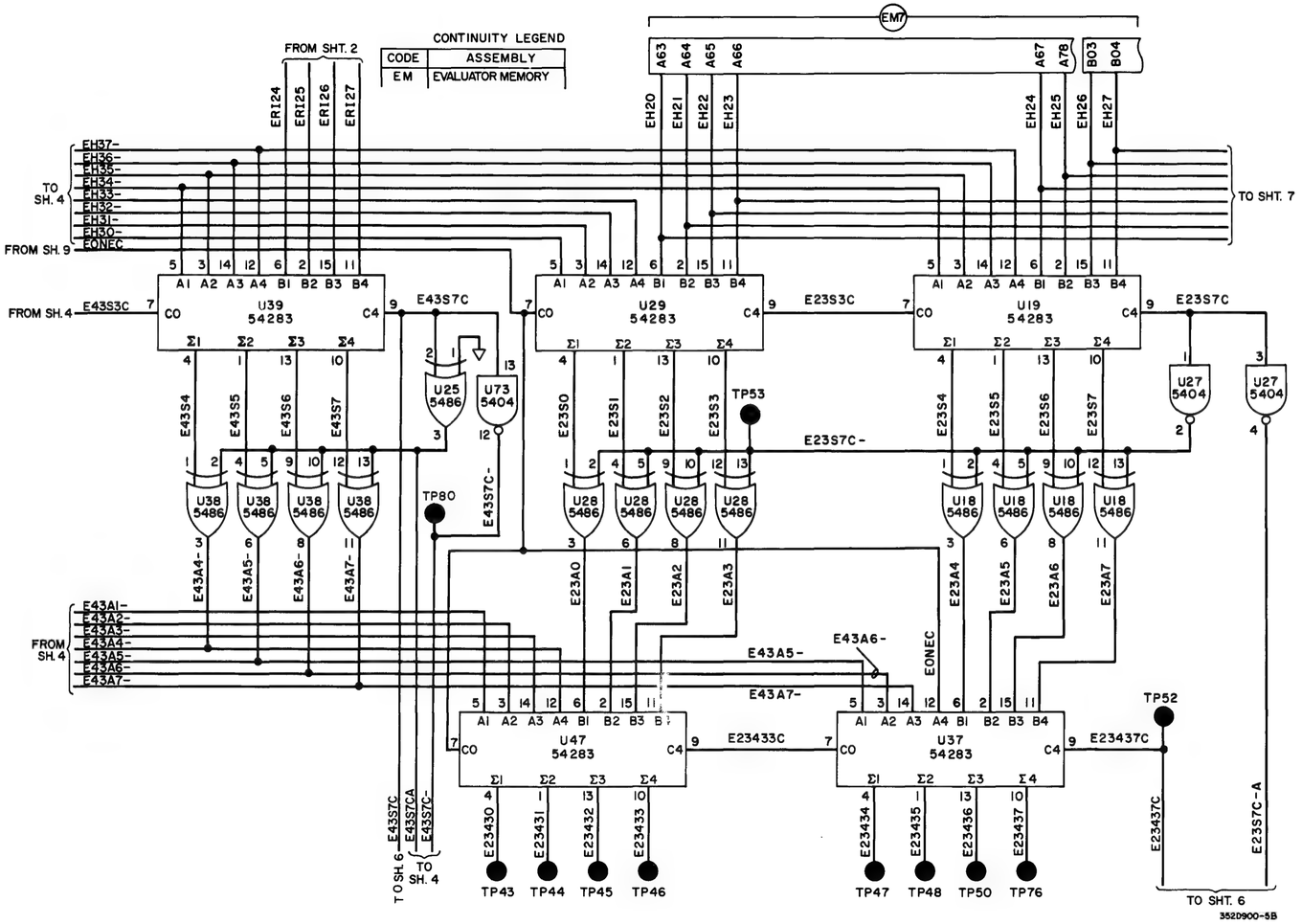
Change 7 FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 2 of 10)



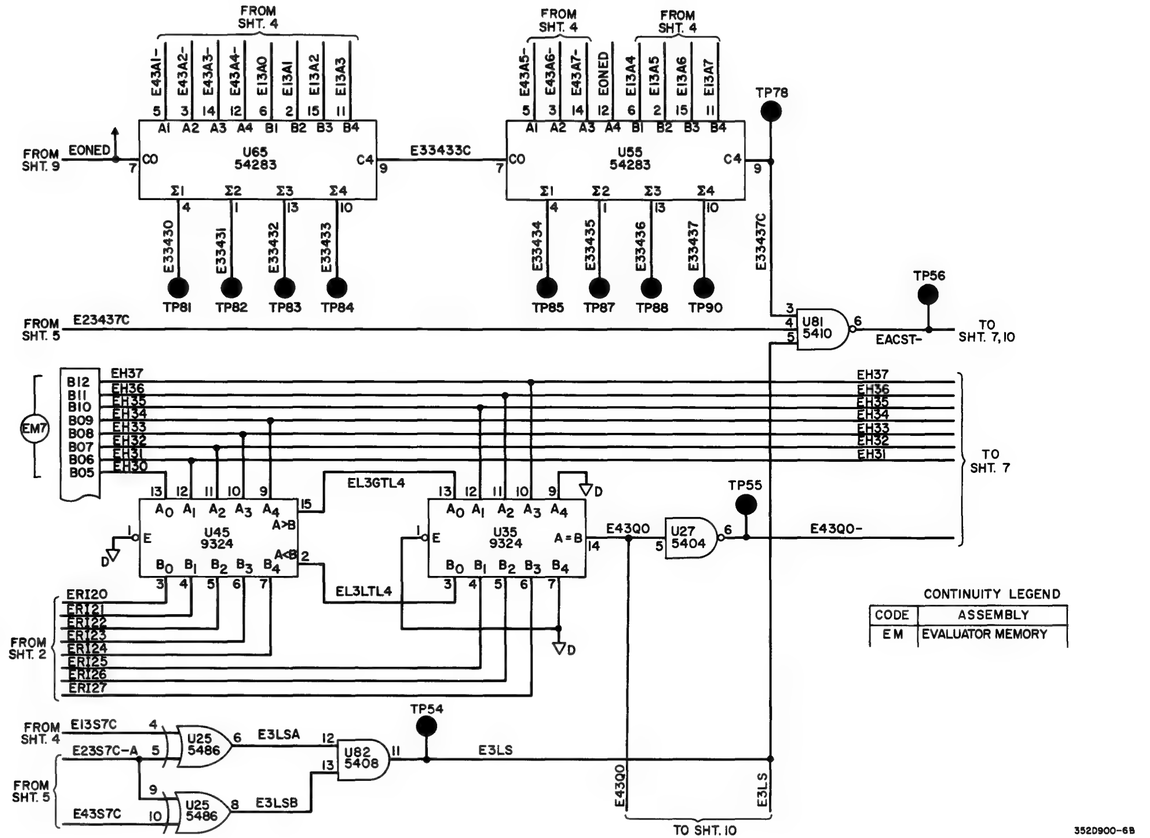
Change 6 FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 3 of 10)



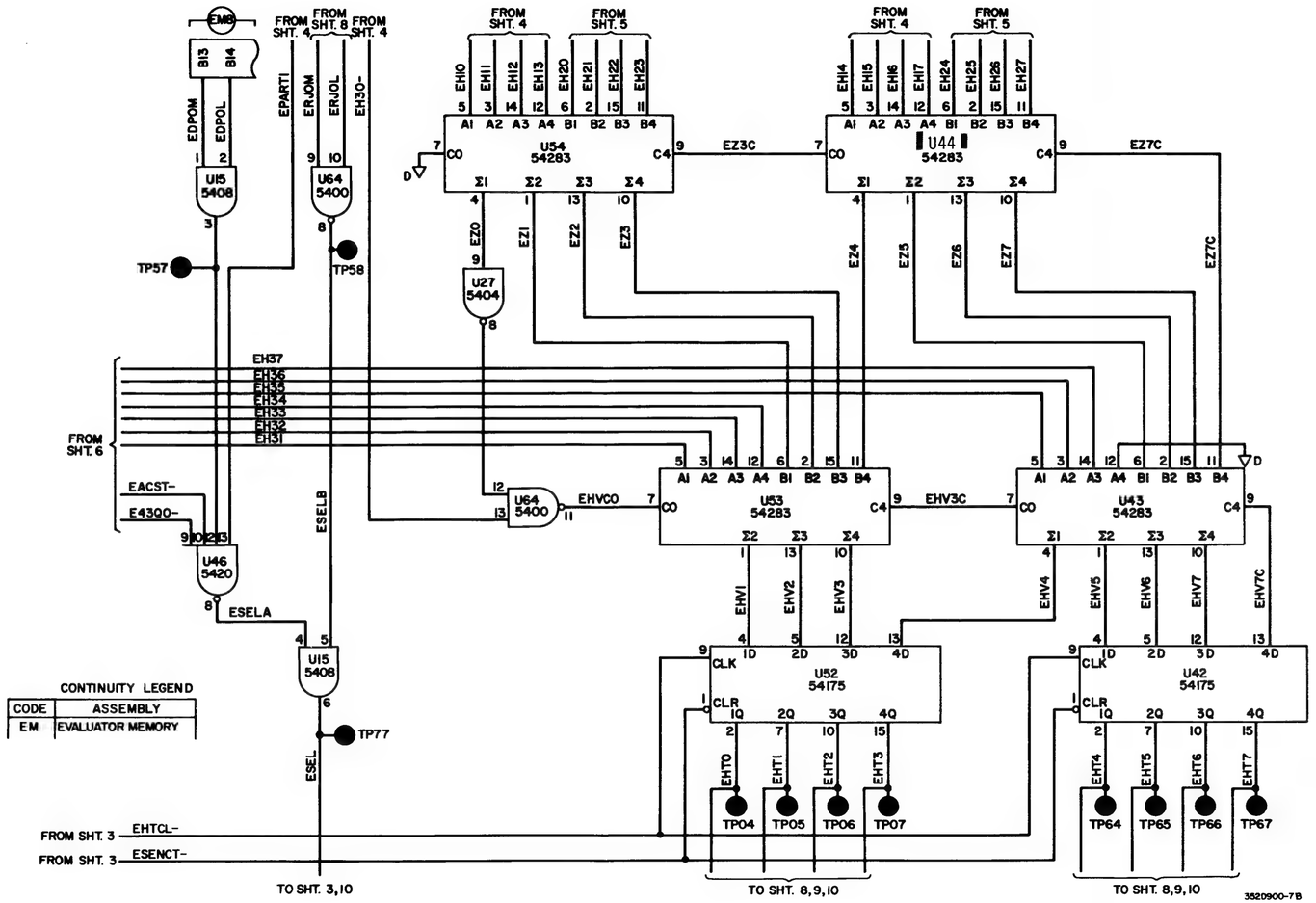
FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 4 of 10)



FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 5 of 10)

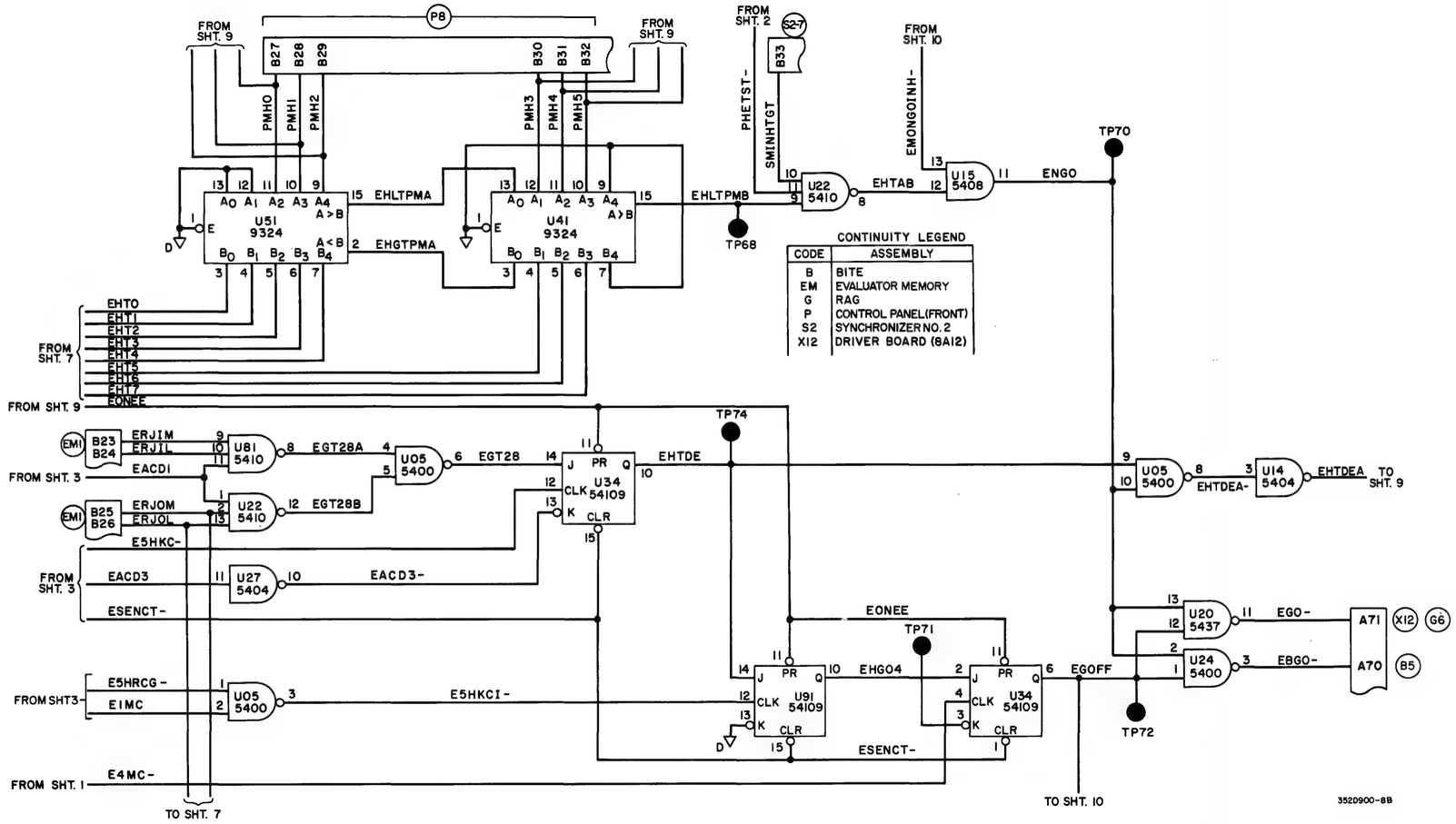


FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 6 of 10)

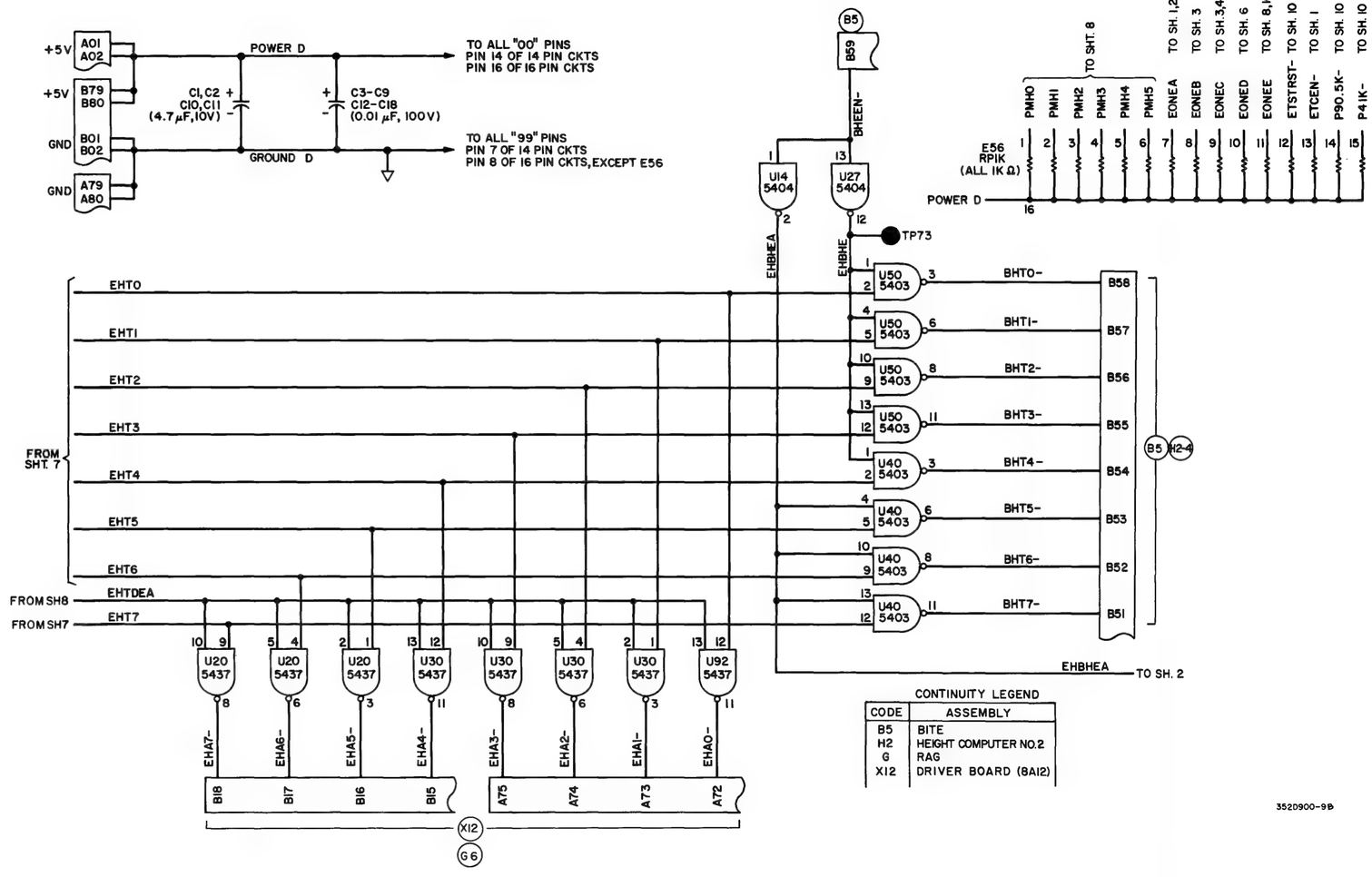


Change 4

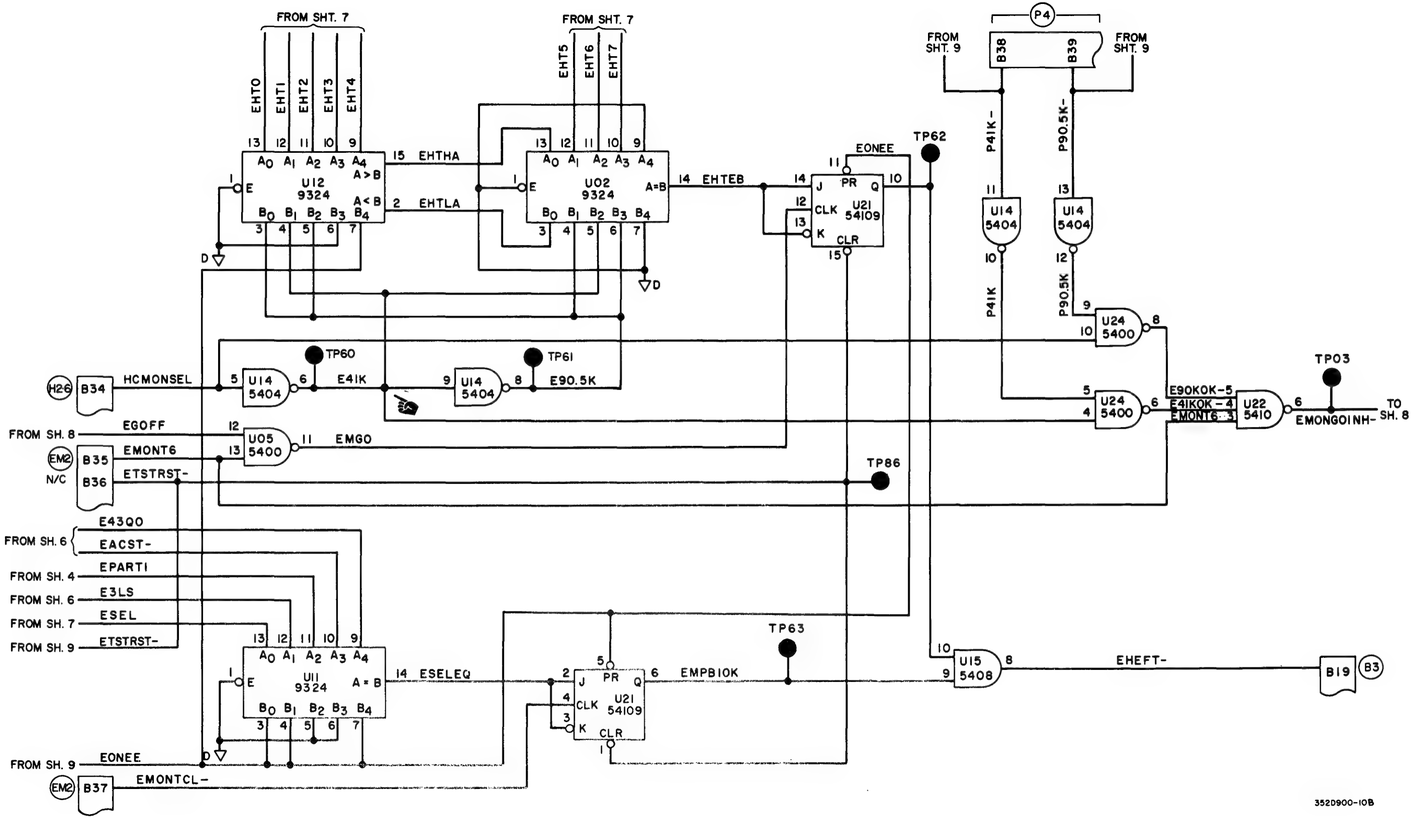
FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 7 of 10)



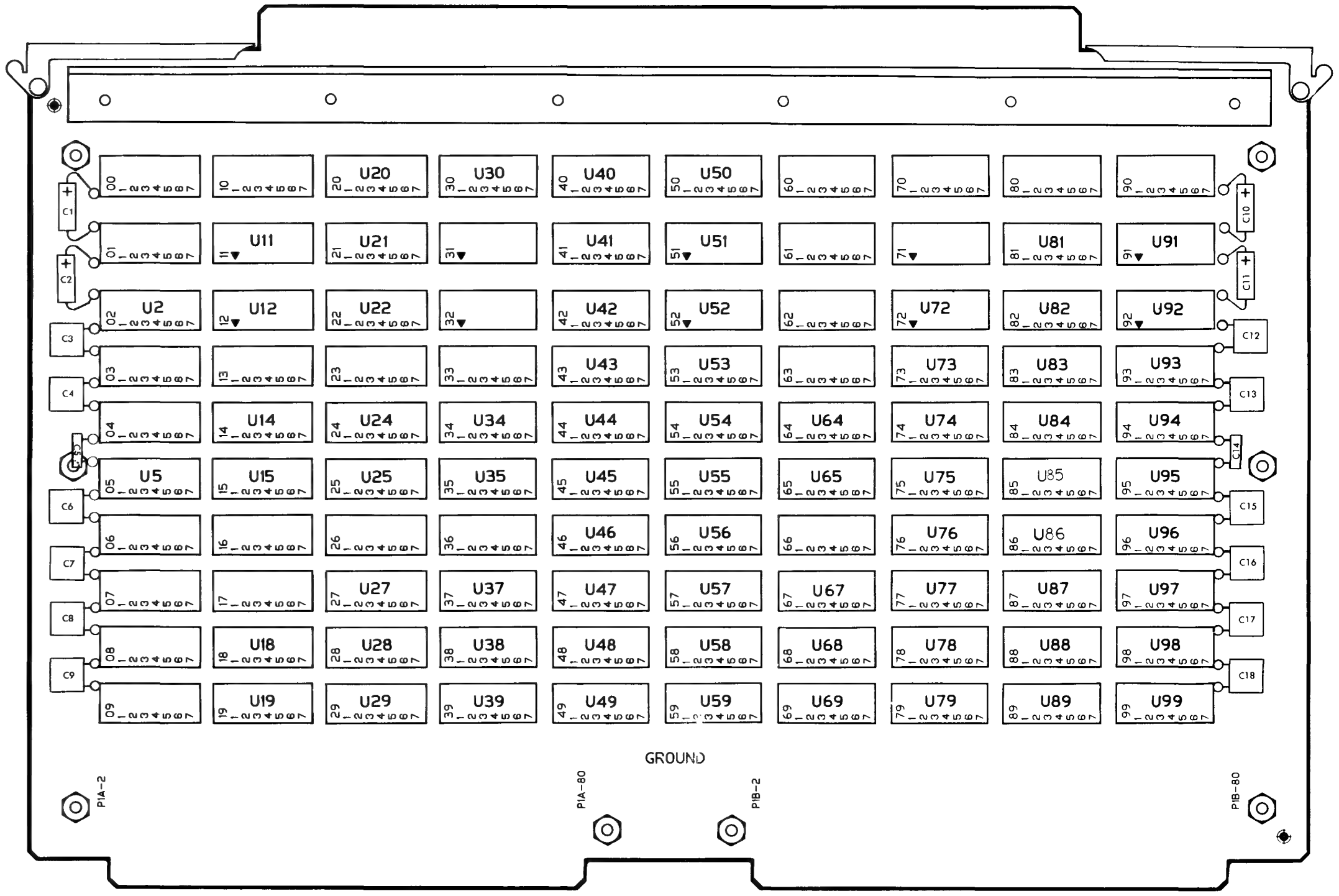
FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 8 of 10)



FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 9 of 10)

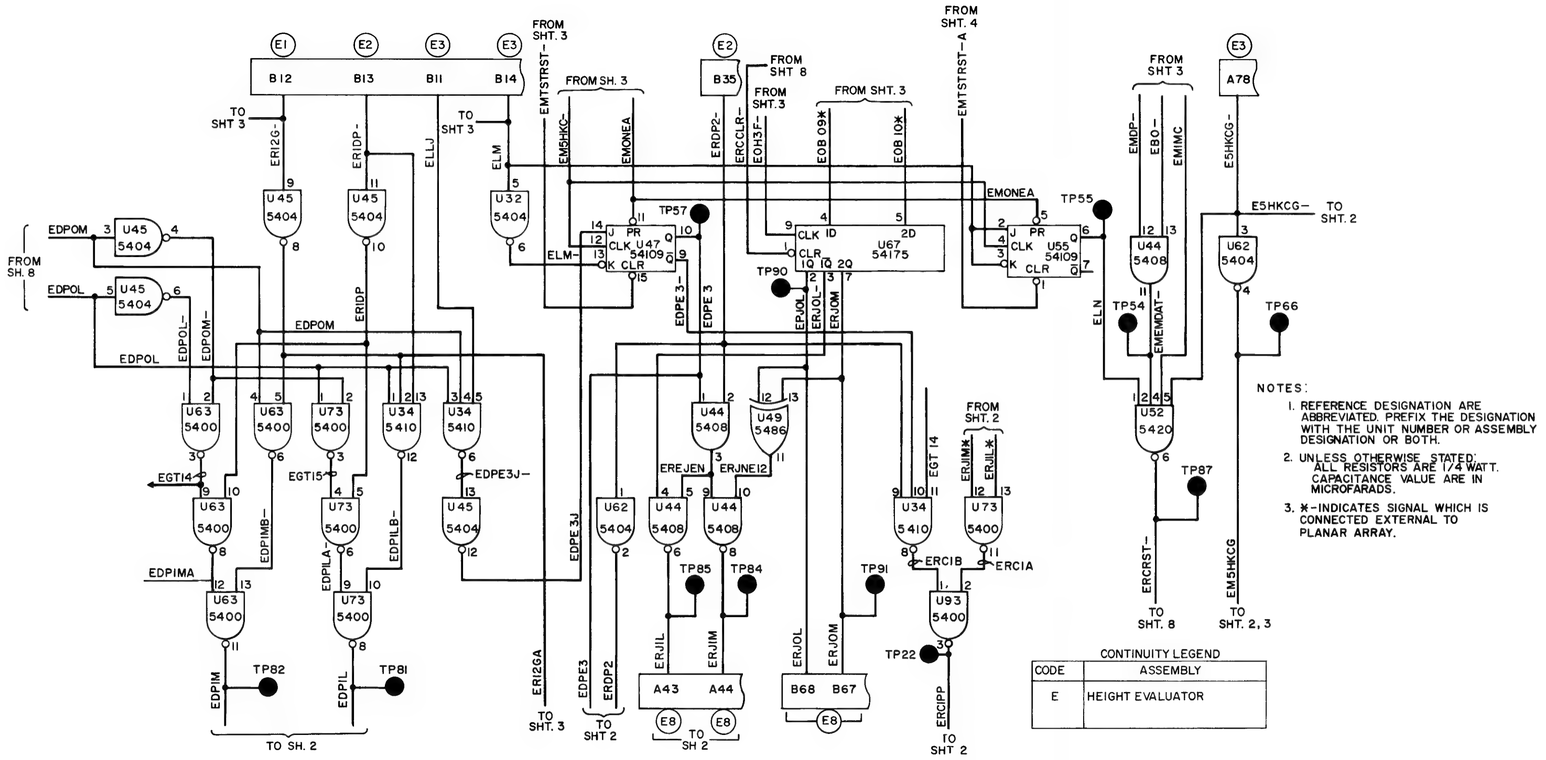


Change 10 FO-57. Height Evaluator Planar Array (352D865) Logic Diagram (Sheet 10 of 10)

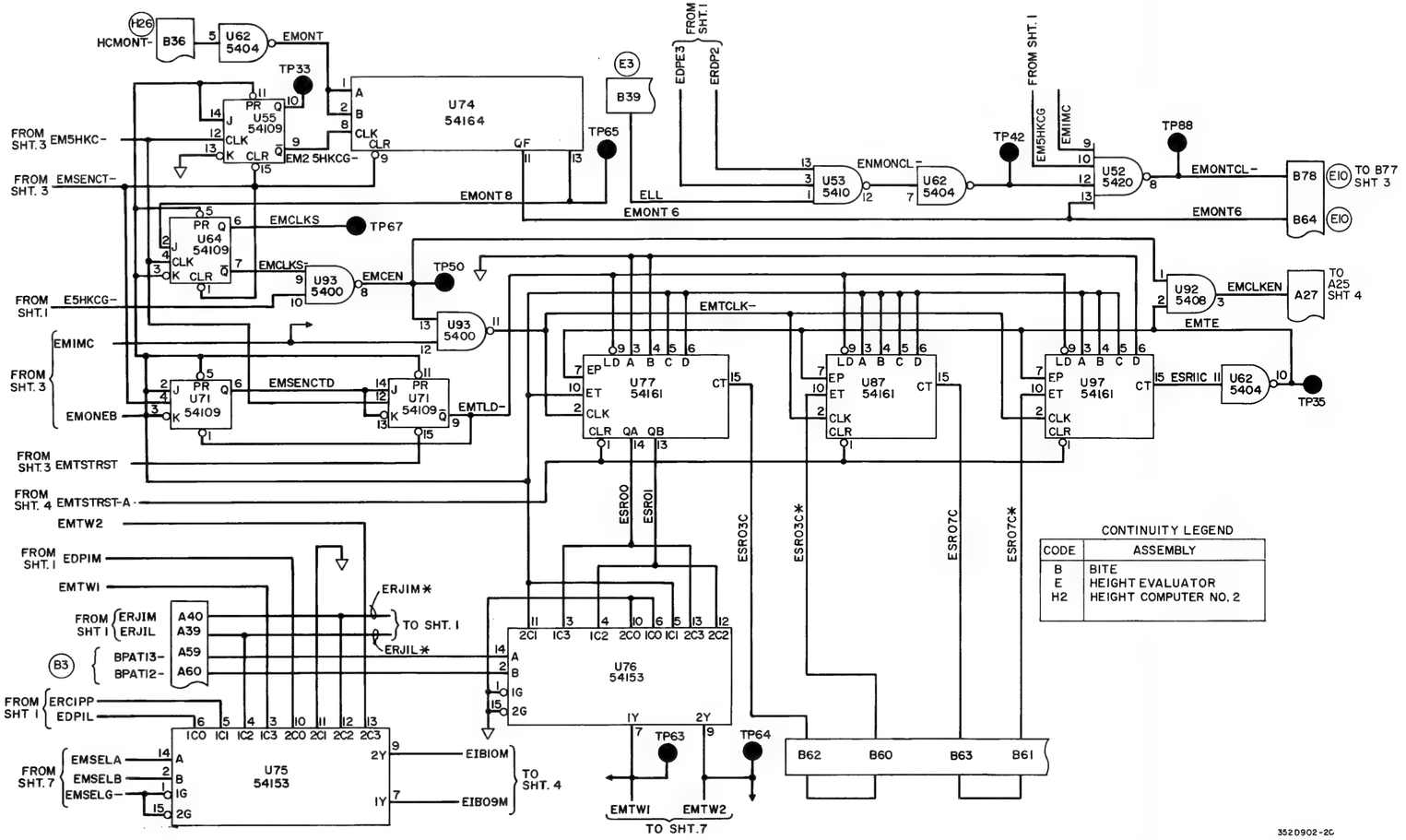


4414A-LD-211A

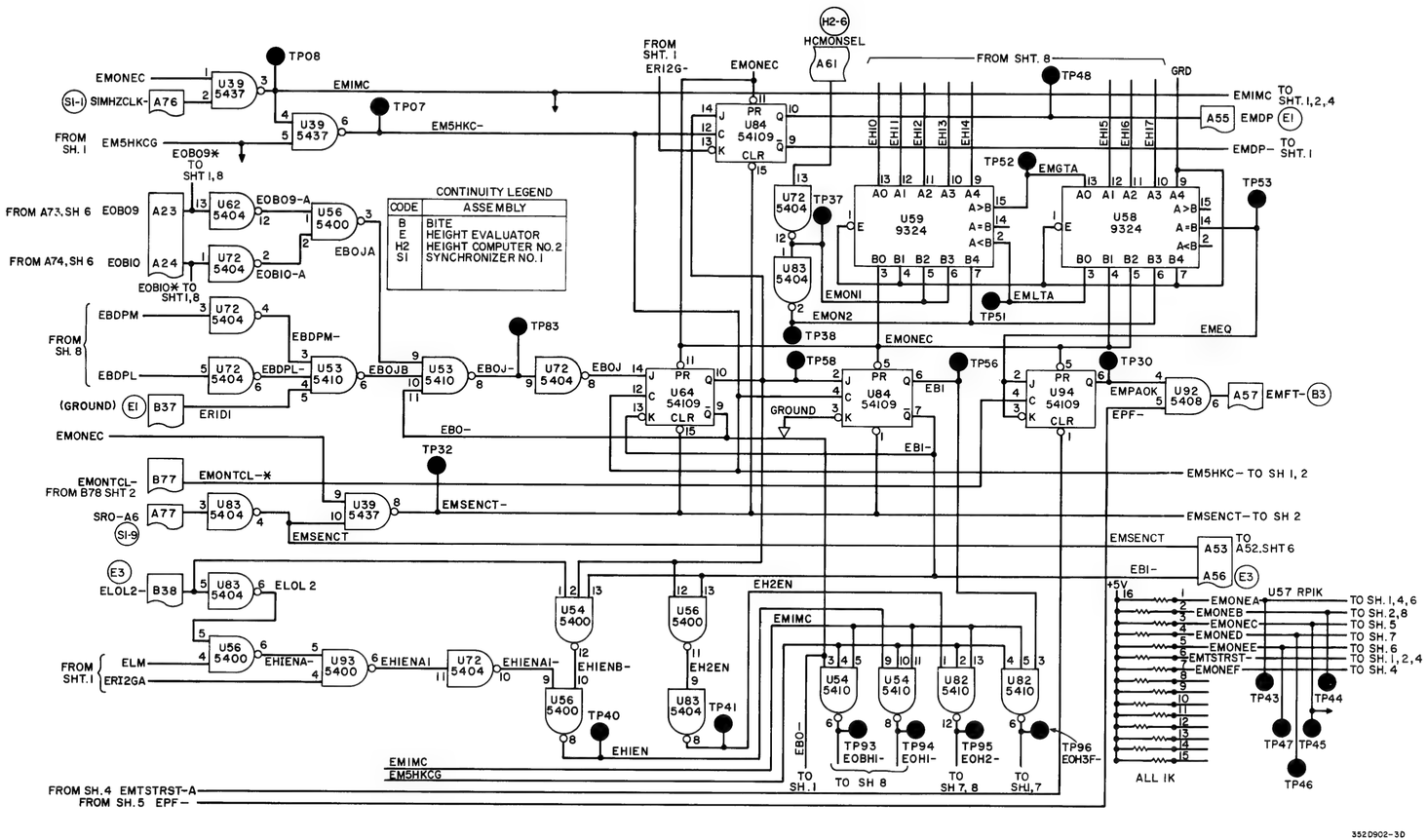
Change 1 FO-57.1. Height Evaluator Planar Array (352D865) Board Component Layout



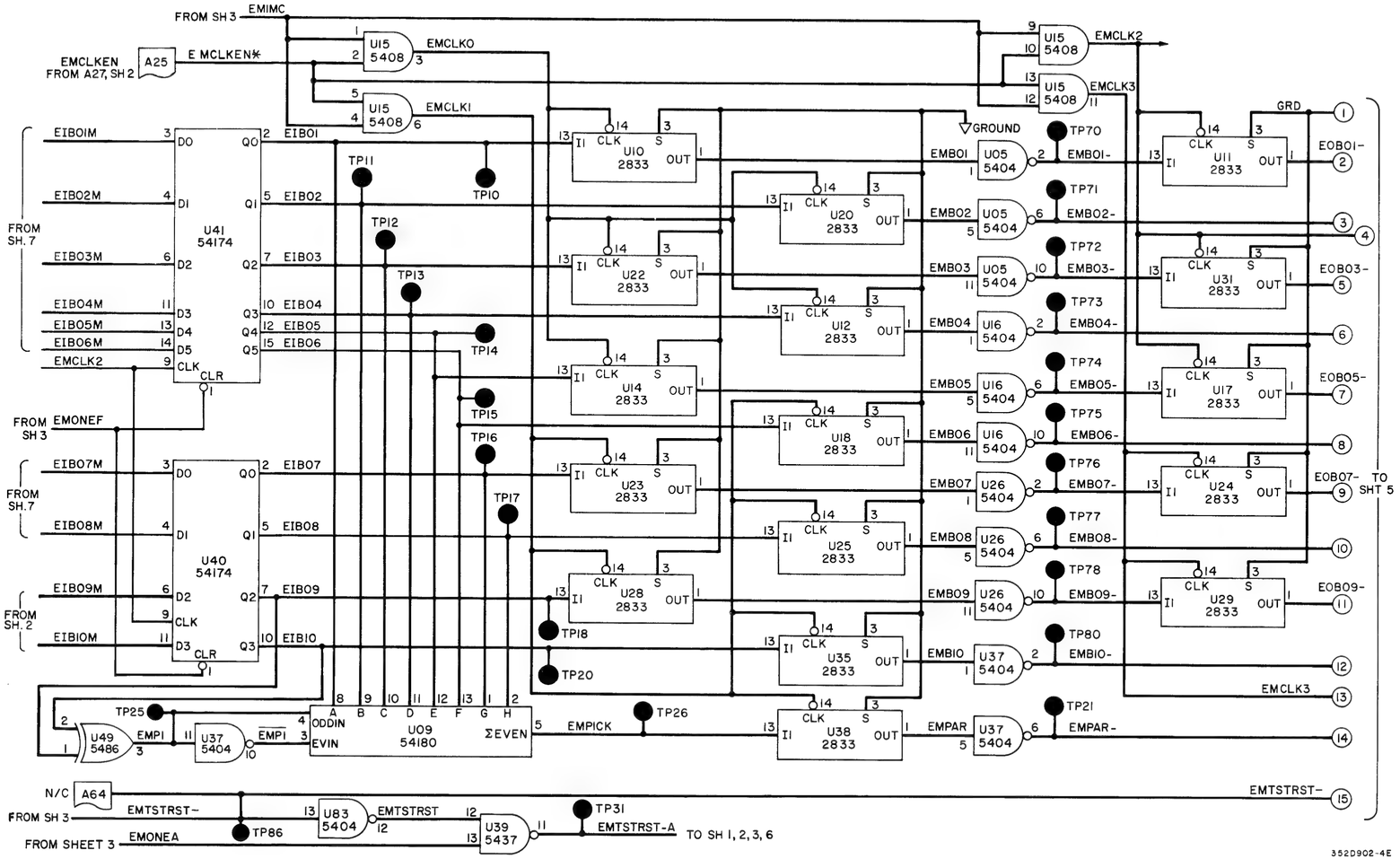
FO-58. Evaluator Memory Planar Array (352D867) Logic Diagram (Sheet 1 of 8)



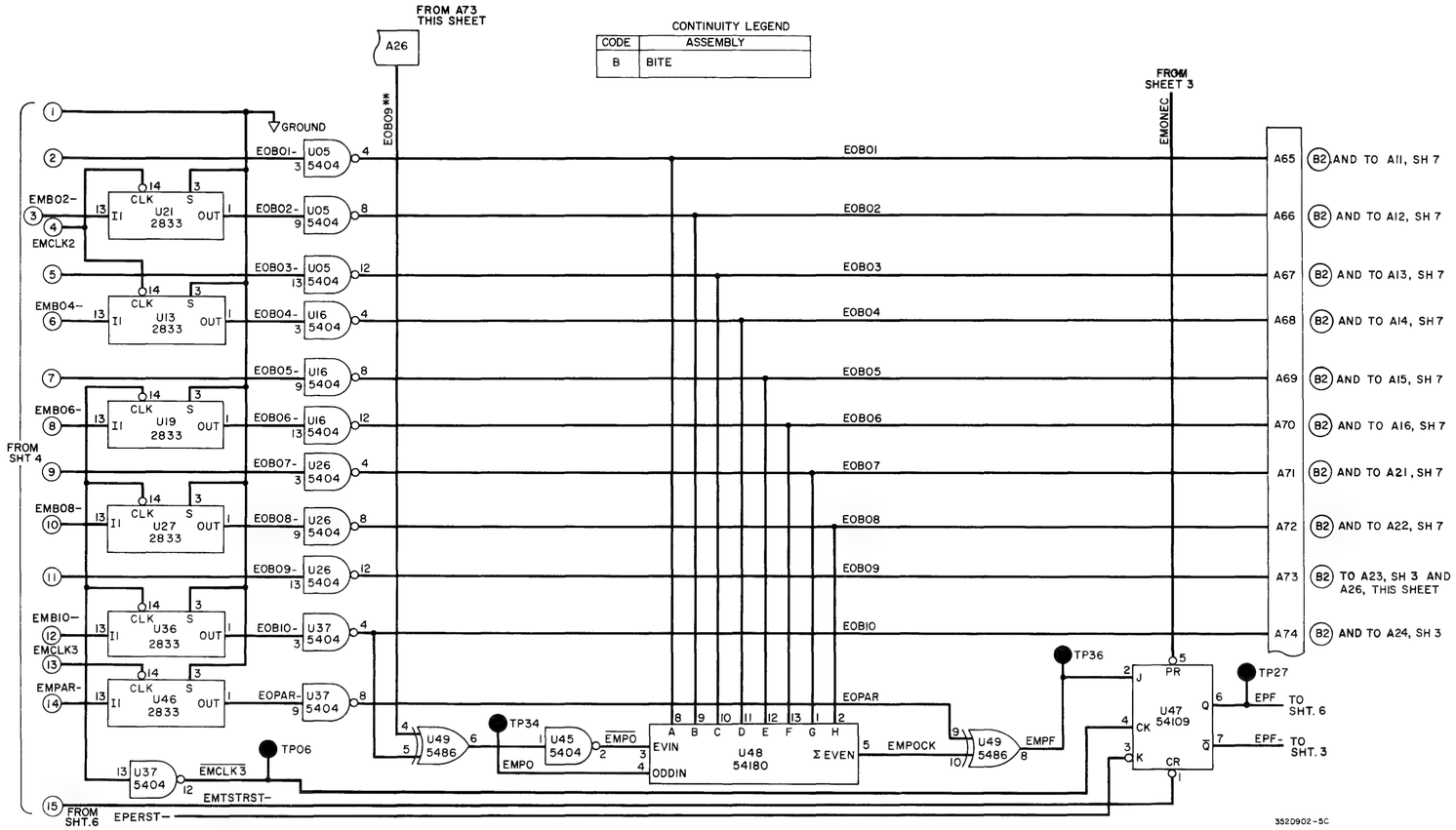
FO-58. Evaluator Memory Planar Array (352D867) Logic Diagram (Sheet 2 of 8)



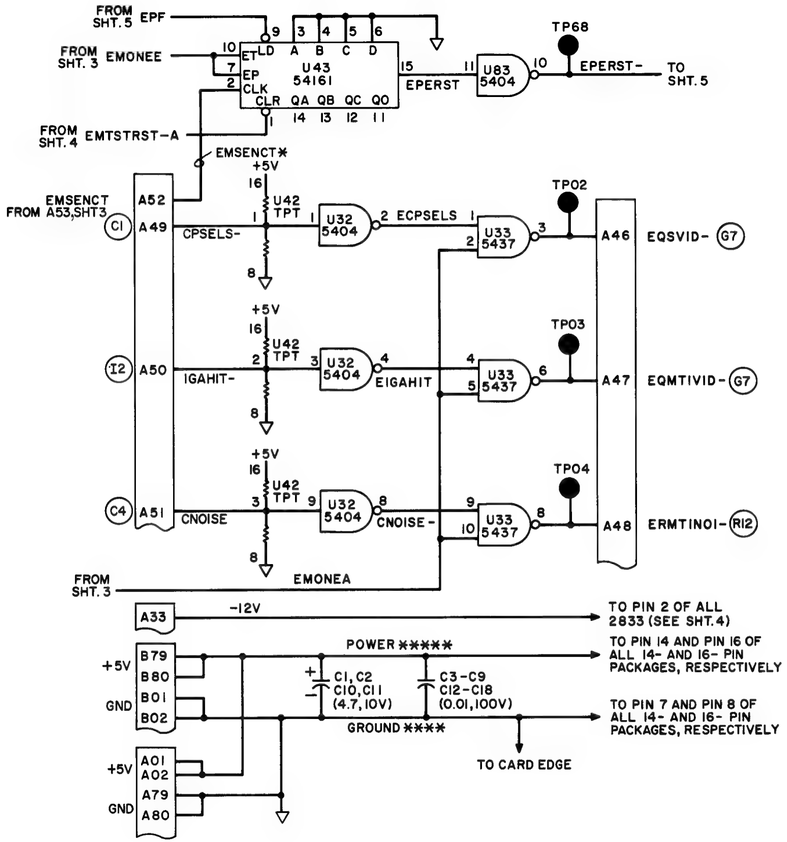
Change 7 FO-58. Evaluator Memory Planar Array (352D867) Logic Diagram (Sheet 3 of 8)



Change 7 FO-58. Evaluator Memory Planar Array (352D867) Logic Diagram (Sheet 4 of 8)



FO-58. Evaluator Memory Planar Array (352D867) Logic Diagram (Sheet 5 of 8)

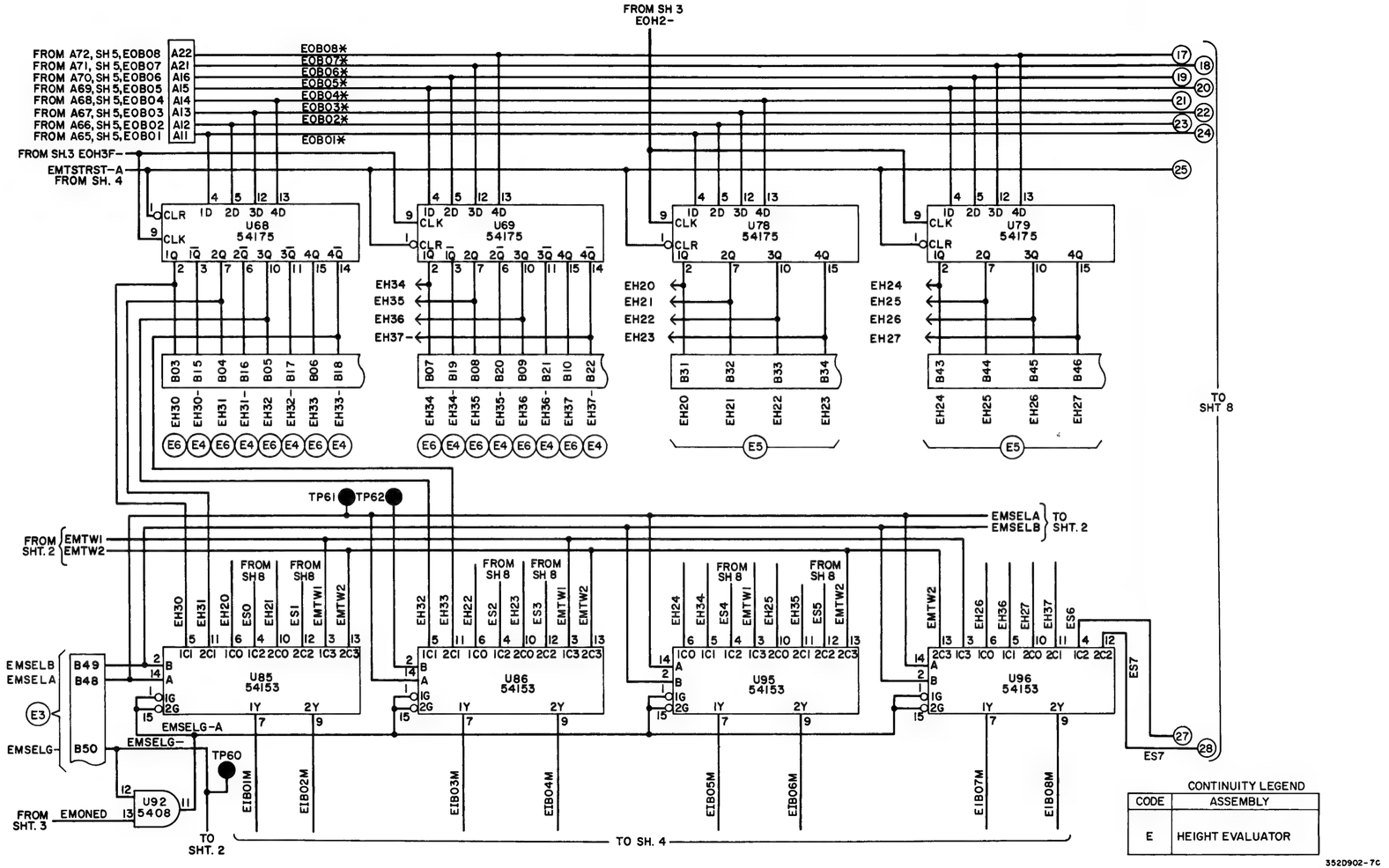


CONTINUITY LEGEND

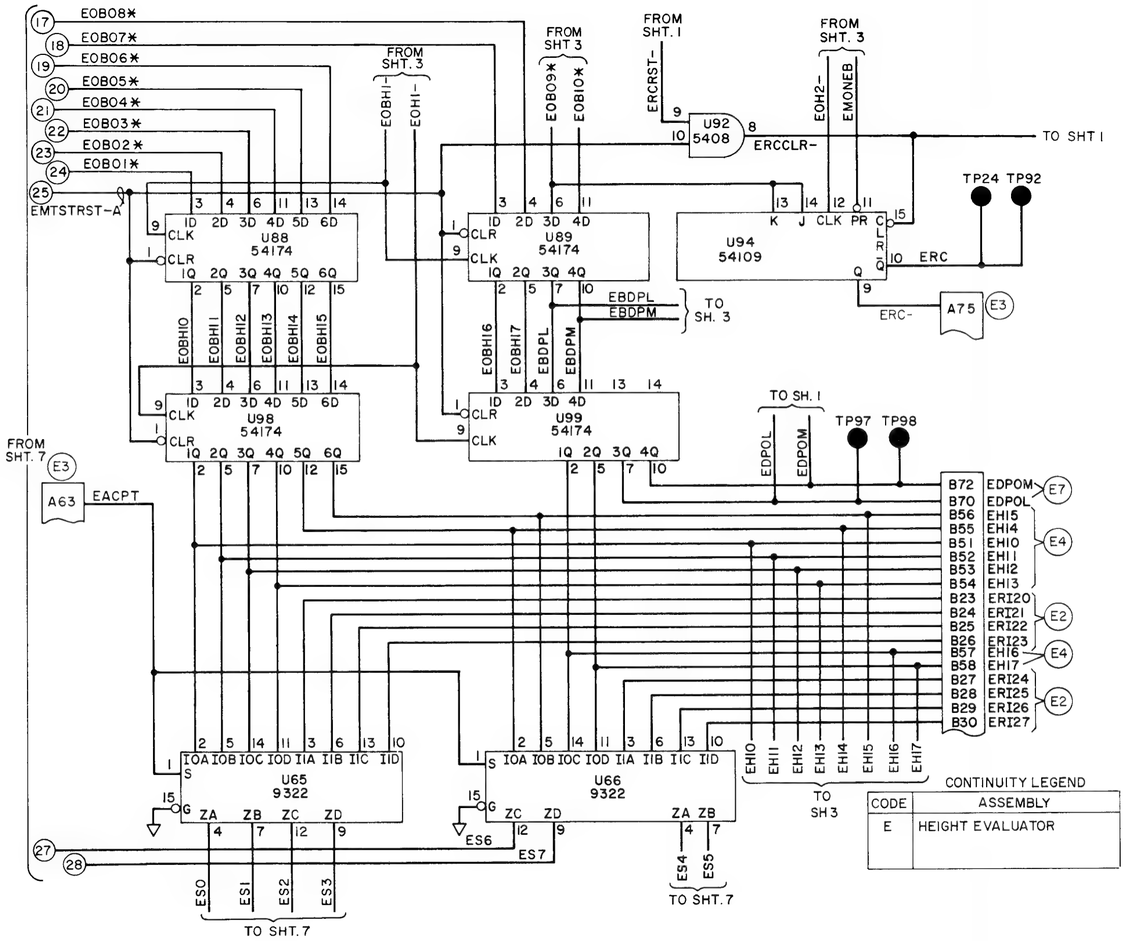
CODE	ASSEMBLY
C	CHANNEL CONTROL
I	INTEGRATOR
G	RAG
R	RECEIVER

352902-6C

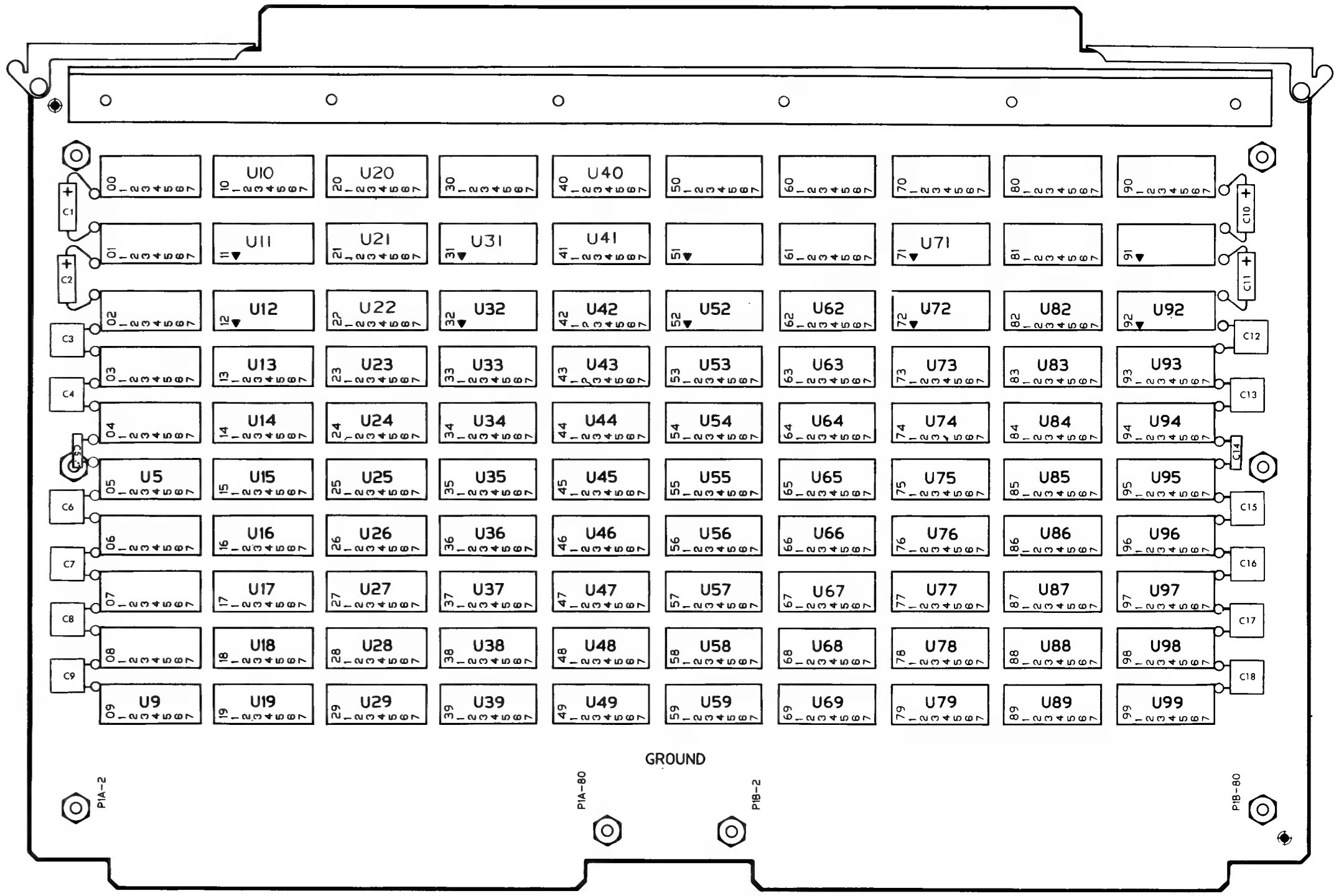
FO-58. Evaluator Memory Planar Array (352D867) Logic Diagram (Sheet 6 of 8)



FO-58. Evaluator Memory Planar Array (352D867) Logic Diagram (Sheet 7 of 8)

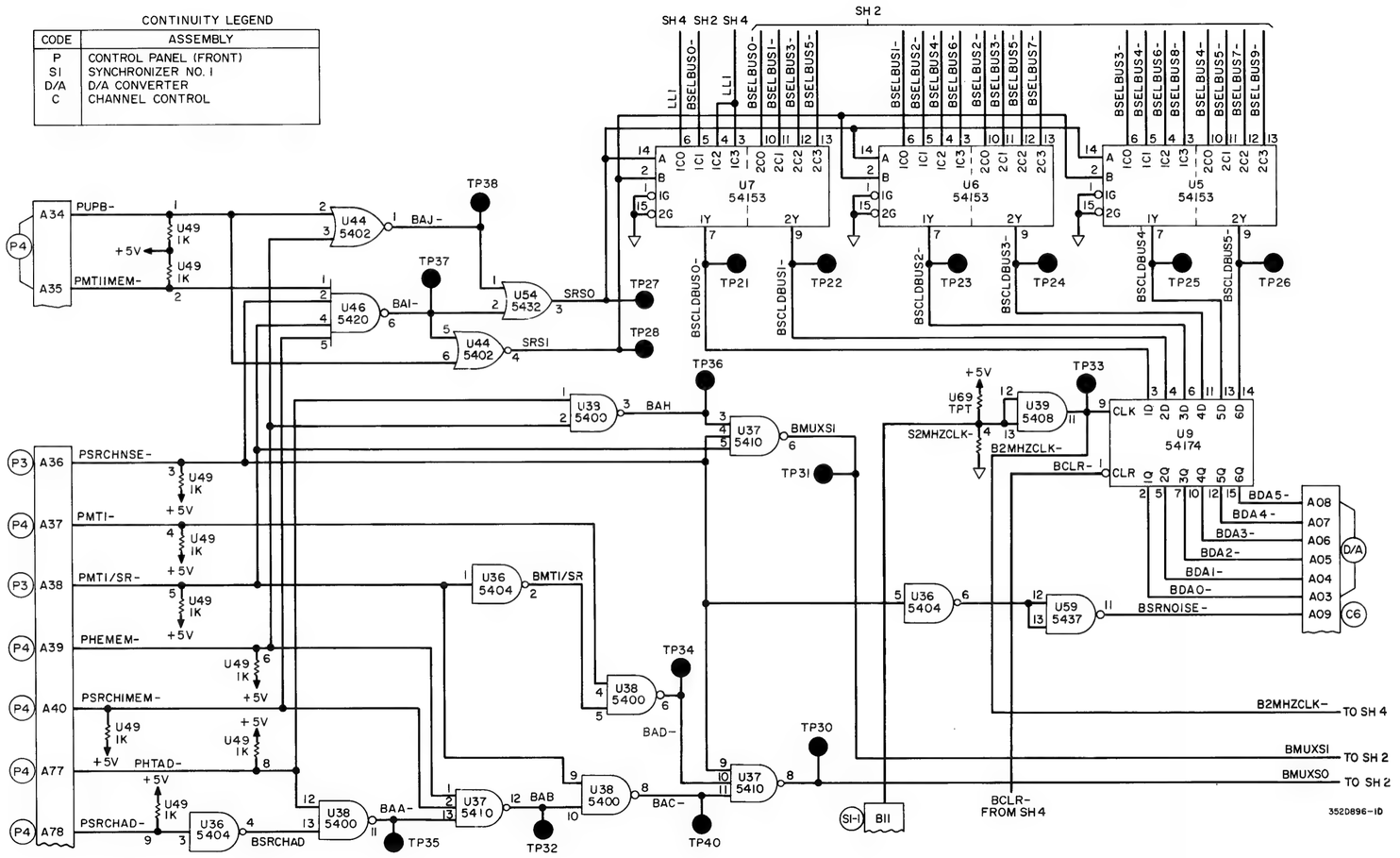


Change 7 FO-58. Evaluator Memory Planar Array (352D867) Logic Diagram (Sheet 8 of 8)

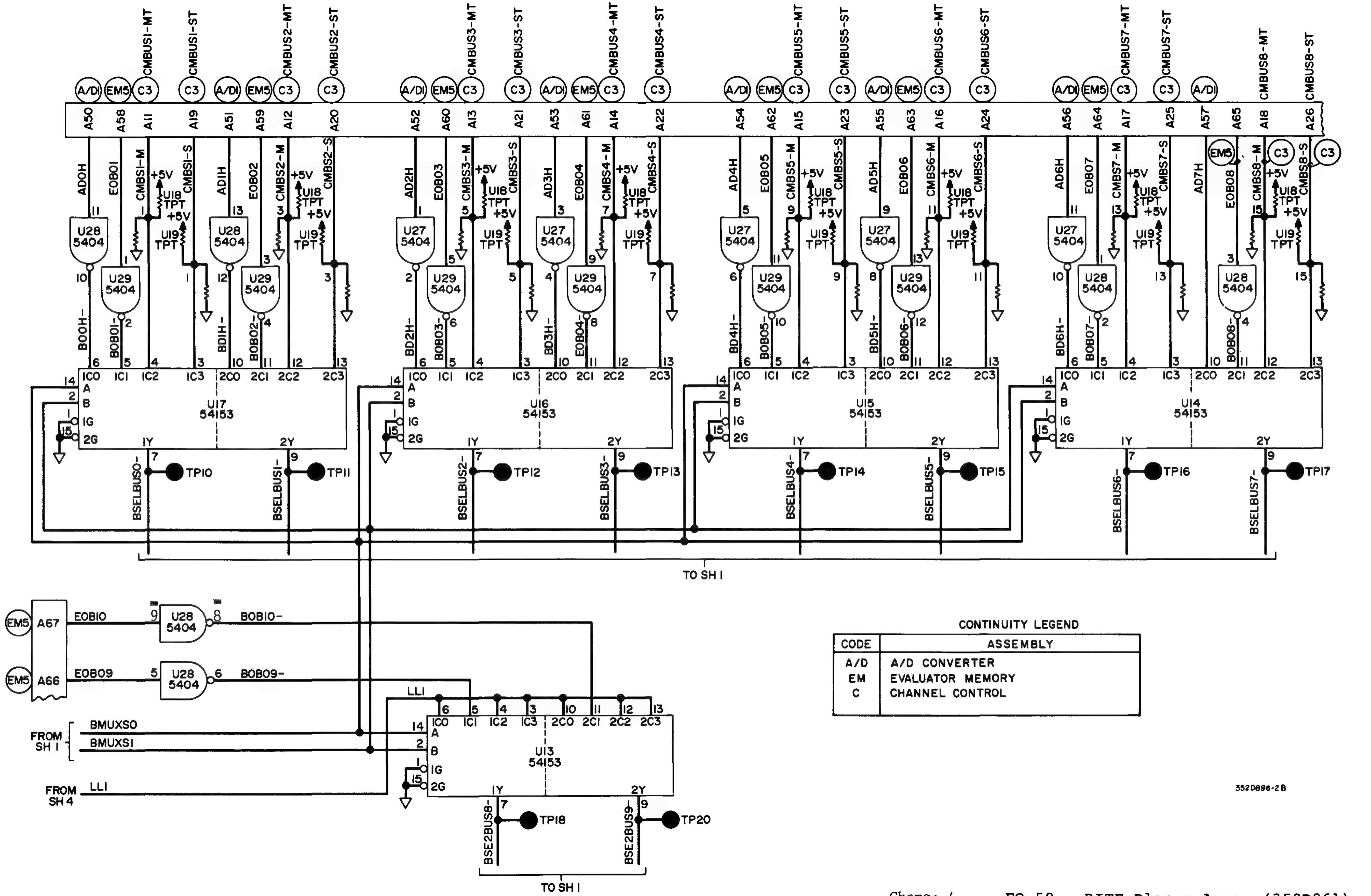


44144A-LD-212A

Change 1 FO-58.1 Evaluator Memory Planar Array (352D867) Board Component Layout



Change 6 FO-59. BITE Planar Array (352D861)
Logic Diagram (Sheet 1 of 5)

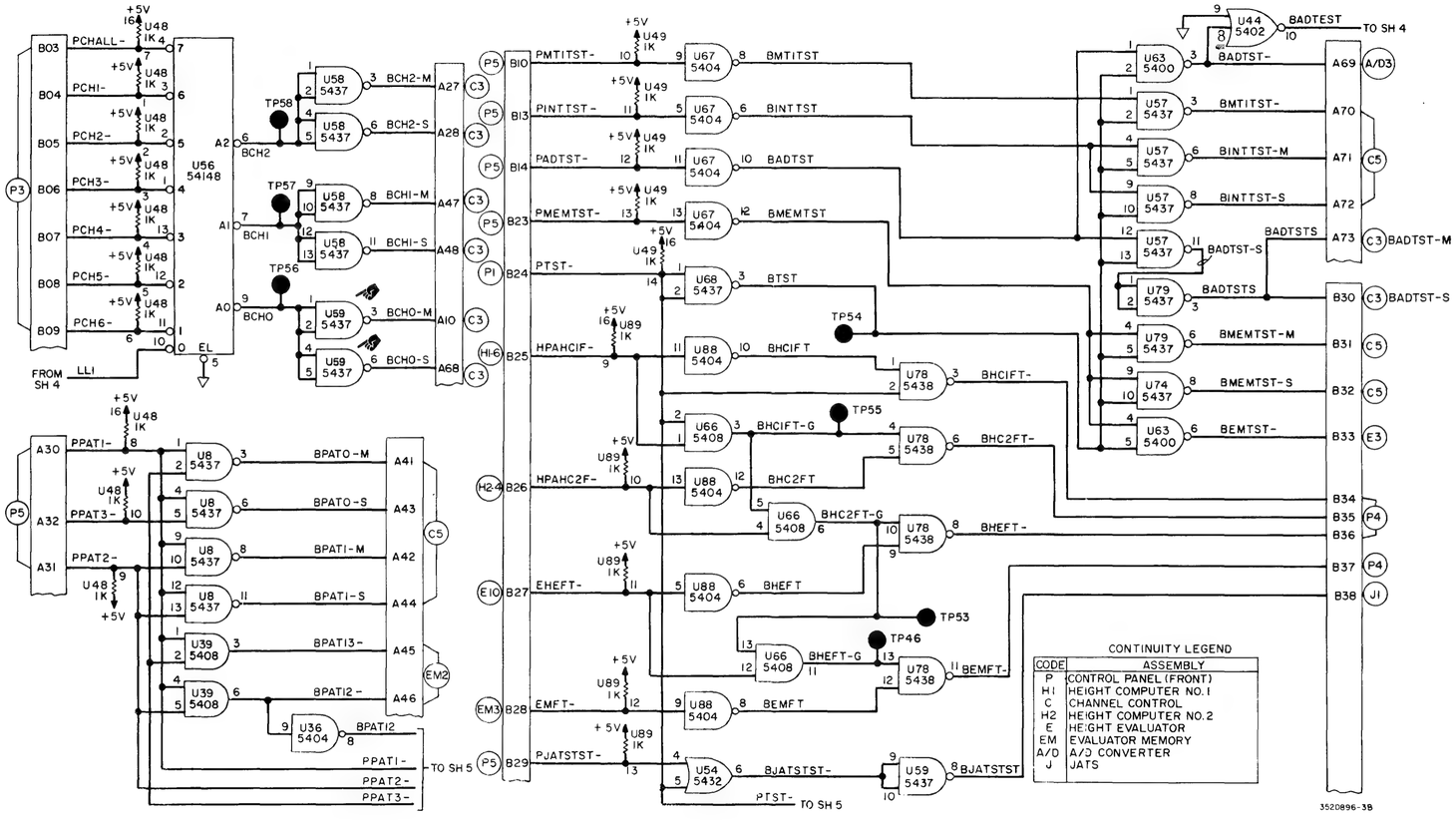


CONTINUITY LEGEND

CODE	ASSEMBLY
A/D	A/D CONVERTER
EM	EVALUATOR MEMORY
C	CHANNEL CONTROL

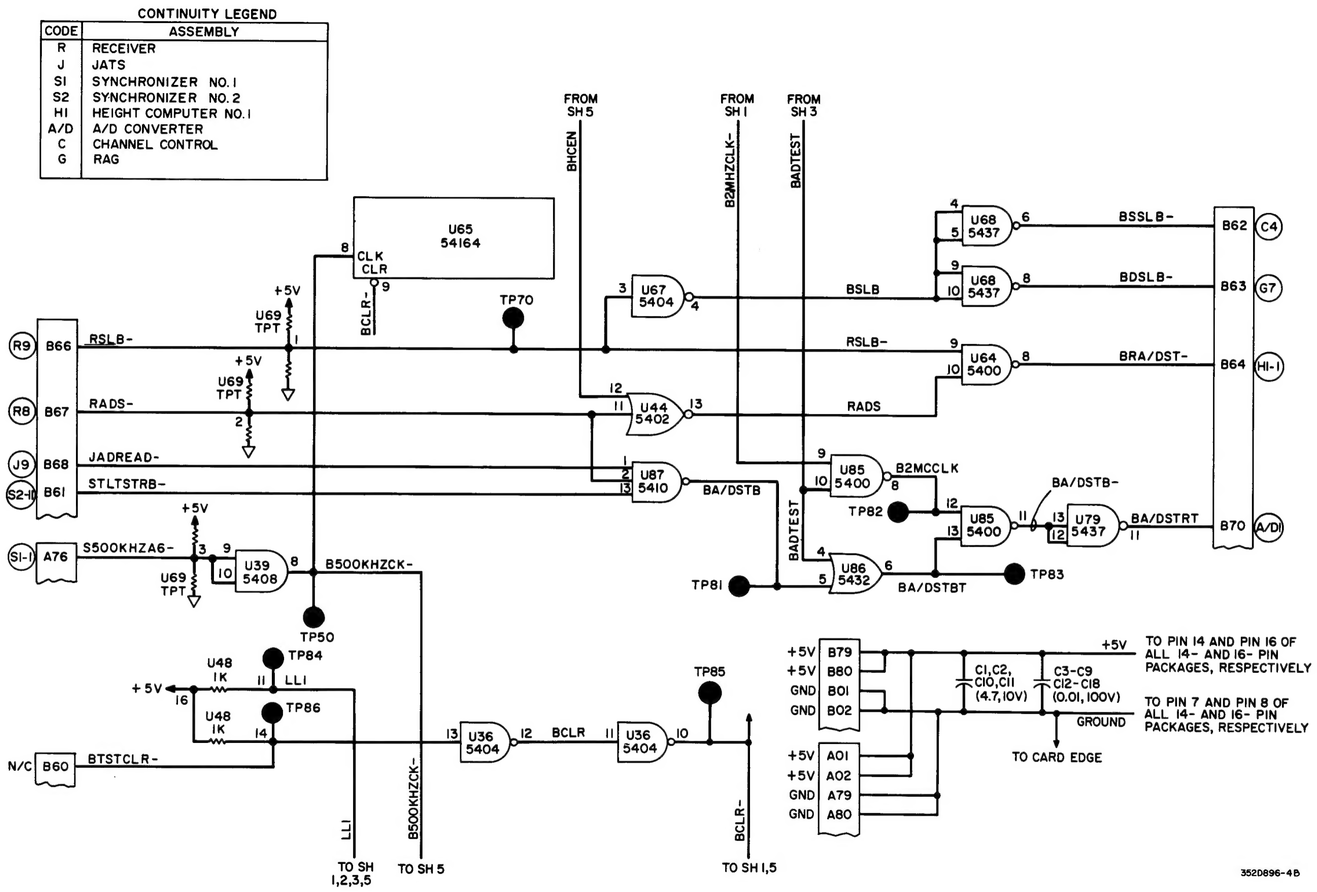
3520896-2B

FO-59. BITE Planar Array (352D861) Logic Diagram (Sheet 2 of 5)

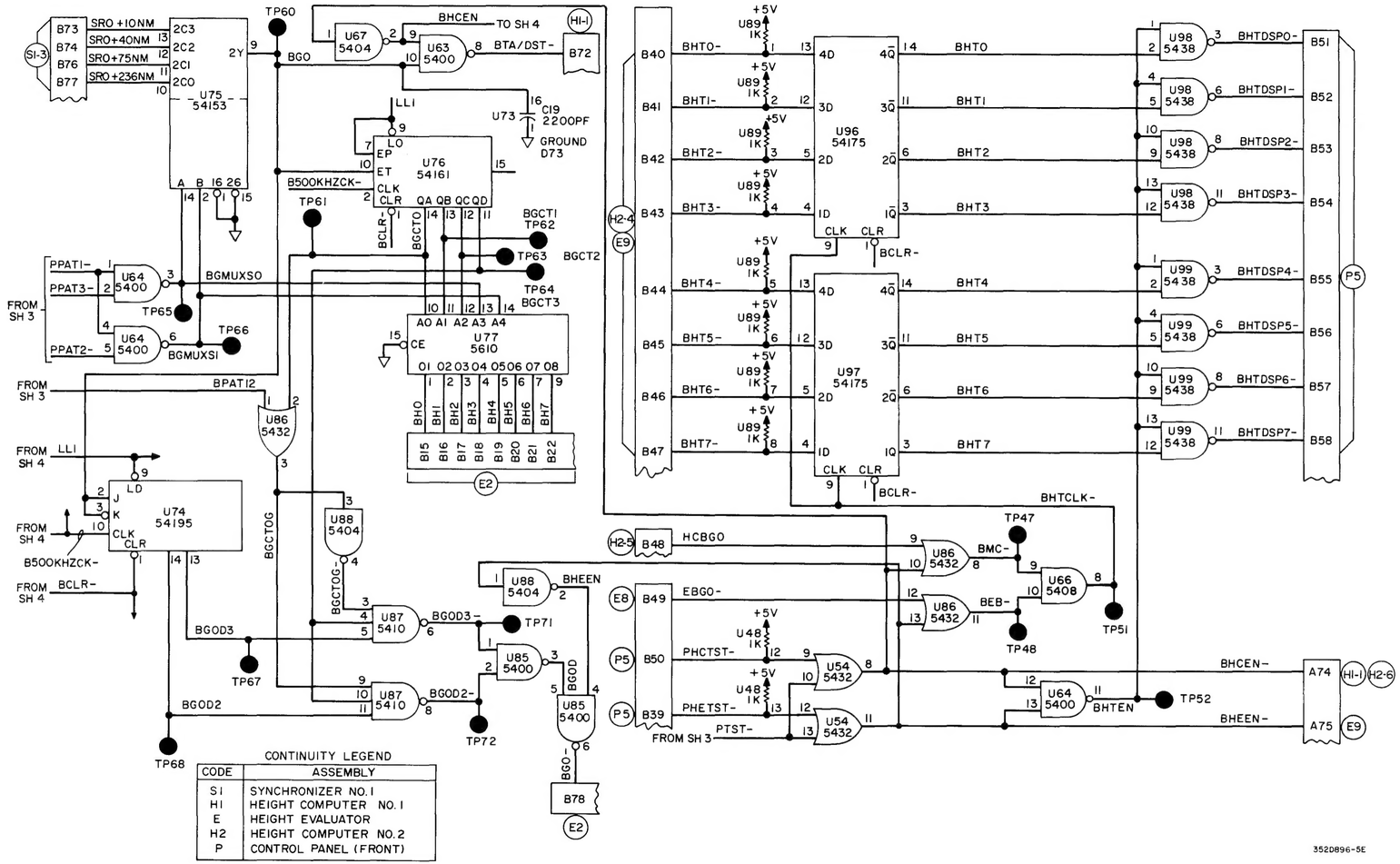


Change 10

FO-59. BITE Planar Array (352D861) Logic Diagram (Sheet 3 of 5)



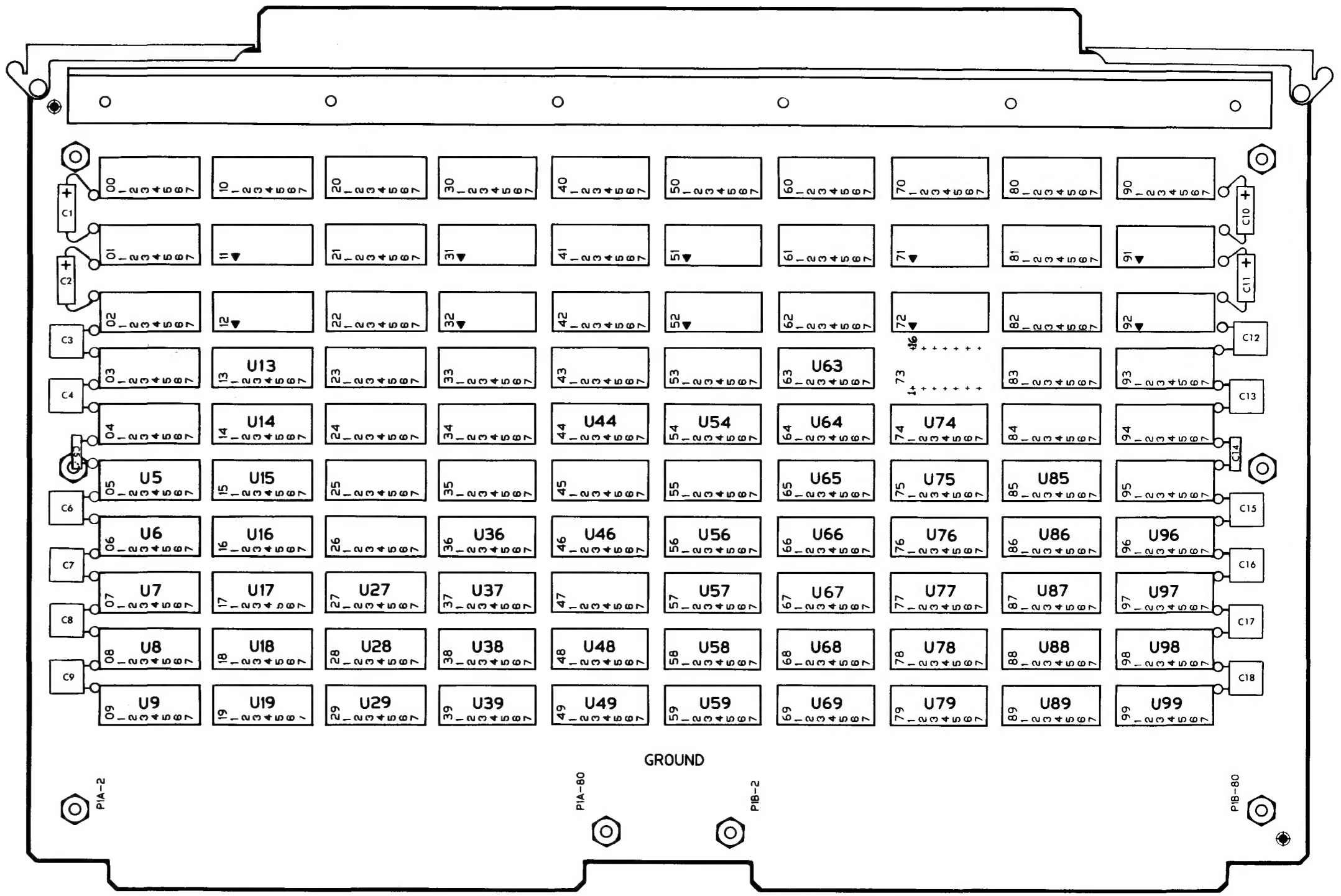
FO-59. BITE Planar Array (352D861) Logic Diagram (Sheet 4 of 5)



CONTINUITY LEGEND	
CODE	ASSEMBLY
S1	SYNCHRONIZER NO.1
HI	HEIGHT COMPUTER NO.1
E	HEIGHT EVALUATOR
H2	HEIGHT COMPUTER NO.2
P	CONTROL PANEL (FRONT)

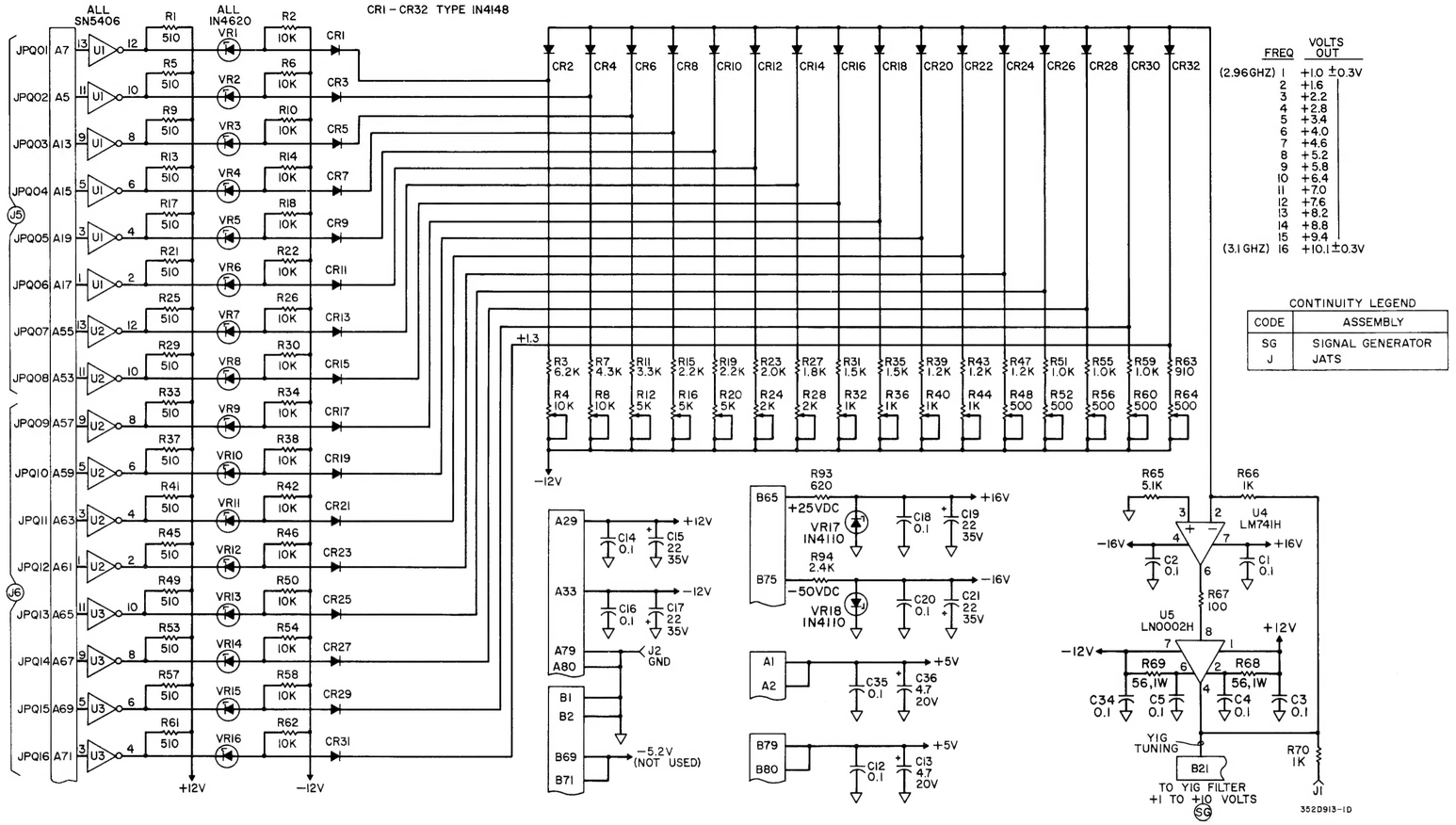
Change 7

FO-59. BITE Planar Array (352D861) Logic Diagram (Sheet 5 of 5)



4414A-LD-213A

Change 1 FO-59.1. BITE Planar Array (352D861) Board Component Layout



Change 7

FO-60. D/A Converter Printed Circuit (352D881) Schematic Diagram (Sheet 1 of 2)